INTERNATIONAL STANDARD

ISO/IEC/IEEE 8802-3

Second edition
2017-03-01

AMENDMENT 8
2018-10

Information technology — Telecommunications and information exchange between systems — Local and metropolitan area networks — Specific requirements —

Part 3: Standard for Ethernet

AMENDMENT 8: Physical layer and management parameters for power over data lines (PoDL) of single balanced twisted-pair ethernet

Technologies de l'information — Télécommunications et échange d'information entre systèmes — Réseaux locaux et métropolitains — Prescriptions spécifiques —

Partie 3: Norme pour Ethernet

AMENDEMENT 8: Titre manque

Reference number
ISO/IEC/IEEE 8802-3:2017/Amd.8:2018(E)

ISO copyright office
CP 401 • Ch. de Blandonnet 8
CH-1214 Vernier, Geneva
Phone: +41 22 749 01 11
Fax: +41 22 749 09 47
Email: copyright@iso.org
Website: www.iso.org

Institute of Electrical and Electronics Engineers, Inc
3 Park Avenue, New York
NY 10016-5997, USA

Email: stds.ipr@ieee.org
Website: www.ieee.org

Published in Switzerland

Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular the different approval criteria needed for the different types of ISO documents should be noted (see www.iso.org/directives).

IEEE Standards documents are developed within the IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (IEEE-SA) Standards Board. The IEEE develops its standards through a consensus development process, approved by the American National Standards Institute, which brings together volunteers representing varied viewpoints and interests to achieve the final product. Volunteers are not necessarily members of the Institute and serve without compensation. While the IEEE administers the process and establishes rules to promote fairness in the consensus development process, the IEEE does not independently evaluate, test, or verify the accuracy of any of the information contained in its standards.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents) or the IEC list of patent declarations received (see http://patents.iec.ch).

Any trade name used in this document is information given for the convenience of users and does not constitute an endorsement.

For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT) see: www.iso.org/iso/foreword.html.

ISO/IEC/IEEE 8802-3:2017/Amd.8 was prepared by the LAN/MAN of the IEEE Computer Society (as IEEE Std 802.3bu-2016) and drafted in accordance with its editorial rules. It was adopted, under the "fast-track procedure" defined in the Partner Standards Development Organization cooperation agreement between ISO and IEEE, by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 6, *Telecommunications and information exchange between systems*.

A list of all parts in the ISO/IEC/IEEE 8802 series can be found on the ISO website.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

IEEE Std 802.3bu™-2016
(Amendment to
IEEE Std 802.3™-2015
as amended by
IEEE Std 802.3bw™-2015,
IEEE Std 802.3by™-2016,
IEEE Std 802.3bq™-2016,
IEEE Std 802.3bp™-2016,
IEEE Std 802.3br™-2016,
IEEE Std 802.3bn™-2016,
and IEEE Std 802.3bz™-2016)

IEEE Standard for Ethernet

Amendment 8: Physical Layer and Management Parameters for Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet

LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 7 December 2016

IEEE-SA Standards Board

Abstract: Specifications and management parameters for the provision of power via a single twisted pair to connected Data Terminal Equipment (DTE) with IEEE 802.3 single balanced twisted-pair interfaces are added by this amendment to IEEE Std 802.3-2015.

Keywords: 100BASE-T1, 1000BASE-T1, Ethernet, IEEE 802.3™, IEEE 802.3bu™, Power over Data Lines, PoDL, PoDL PD, PoDL PSE

Acknowledgments: Portions of the material contained herein are reprinted with permission from Maxim Integrated Products, Inc., DS18B20 “Programmable Resolution 1-Wire Digital Thermometer” Data Sheet, Rev. 042208, (C) 2008.

The Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue, New York, NY 10016-5997, USA

Print: ISBN 978-1-5044-3727-1 STD22416
PDF: ISBN 978-1-5044-3728-8 STDPD22416

Important Notices and Disclaimers Concerning IEEE Standards Documents

IEEE documents are made available for use subject to important notices and legal disclaimers. These notices and disclaimers, or a reference to this page, appear in all standards and may be found under the heading "Important Notice" or "Important Notices and Disclaimers Concerning IEEE Standards Documents."

Notice and Disclaimer of Liability Concerning the Use of IEEE Standards Documents

IEEE Standards documents (standards, recommended practices, and guides), both full-use and trial-use, are developed within IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association ("IEEE-SA") Standards Board. IEEE ("the Institute") develops its standards through a consensus development process, approved by the American National Standards Institute ("ANSI"), which brings together volunteers representing varied viewpoints and interests to achieve the final product. Volunteers are not necessarily members of the Institute and participate without compensation from IEEE. While IEEE administers the process and establishes rules to promote fairness in the consensus development process, IEEE does not independently evaluate, test, or verify the accuracy of any of the information or the soundness of any judgments contained in its standards.

IEEE does not warrant or represent the accuracy or content of the material contained in its standards, and expressly disclaims all warranties (express, implied and statutory) not included in this or any other document relating to the standard, including, but not limited to, the warranties of: merchantability; fitness for a particular purpose; non-infringement; and quality, accuracy, effectiveness, currency, or completeness of material. In addition, IEEE disclaims any and all conditions relating to: results; and workmanlike effort. IEEE standards documents are supplied "AS IS" and "WITH ALL FAULTS."

Use of an IEEE standard is wholly voluntary. The existence of an IEEE standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard.

In publishing and making its standards available, IEEE is not suggesting or rendering professional or other services for, or on behalf of, any person or entity nor is IEEE undertaking to perform any duty owed by any other person or entity to another. Any person utilizing any IEEE Standards document, should rely upon his or her own independent judgment in the exercise of reasonable care in any given circumstances or, as appropriate, seek the advice of a competent professional in determining the appropriateness of a given IEEE standard.

IN NO EVENT SHALL IEEE BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO: PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE PUBLICATION, USE OF, OR RELIANCE UPON ANY STANDARD, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE AND REGARDLESS OF WHETHER SUCH DAMAGE WAS FORESEEABLE.

Translations

The IEEE consensus development process involves the review of documents in English only. In the event that an IEEE standard is translated, only the English version published by IEEE should be considered the approved IEEE standard.

Official statements

A statement, written or oral, that is not processed in accordance with the IEEE-SA Standards Board Operations Manual shall not be considered or inferred to be the official position of IEEE or any of its committees and shall not be considered to be, or be relied upon as, a formal position of IEEE. At lectures, symposia, seminars, or educational courses, an individual presenting information on IEEE standards shall make it clear that his or her views should be considered the personal views of that individual rather than the formal position of IEEE.

Comments on standards

Comments for revision of IEEE Standards documents are welcome from any interested party, regardless of membership affiliation with IEEE. However, IEEE does not provide consulting information or advice pertaining to IEEE Standards documents. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Since IEEE standards represent a consensus of concerned interests, it is important that any responses to comments and questions also receive the concurrence of a balance of interests. For this reason, IEEE and the members of its societies and Standards Coordinating Committees are not able to provide an instant response to comments or questions except in those cases where the matter has previously been addressed. For the same reason, IEEE does not respond to interpretation requests. Any person who would like to participate in revisions to an IEEE standard is welcome to join the relevant IEEE working group.

Comments on standards should be submitted to the following address:

Secretary, IEEE-SA Standards Board
445 Hoes Lane
Piscataway, NJ 08854 USA

Laws and regulations

Users of IEEE Standards documents should consult all applicable laws and regulations. Compliance with the provisions of any IEEE Standards document does not imply compliance to any applicable regulatory requirements. Implementers of the standard are responsible for observing or referring to the applicable regulatory requirements. IEEE does not, by the publication of its standards, intend to urge action that is not in compliance with applicable laws, and these documents may not be construed as doing so.

Copyrights

IEEE draft and approved standards are copyrighted by IEEE under U.S. and international copyright laws. They are made available by IEEE and are adopted for a wide variety of both public and private uses. These include both use, by reference, in laws and regulations, and use in private self-regulation, standardization, and the promotion of engineering practices and methods. By making these documents available for use and adoption by public authorities and private users, IEEE does not waive any rights in copyright to the documents.

Photocopies

Subject to payment of the appropriate fee, IEEE will grant users a limited, non-exclusive license to photocopy portions of any individual standard for company or organizational internal use or individual, non-commercial use only. To arrange for payment of licensing fees, please contact Copyright Clearance Center, Customer Service, 222 Rosewood Drive, Danvers, MA 01923 USA; +1 978 750 8400. Permission to photocopy portions of any individual standard for educational classroom use can also be obtained through the Copyright Clearance Center.

Updating of IEEE Standards documents

Users of IEEE Standards documents should be aware that these documents may be superseded at any time by the issuance of new editions or may be amended from time to time through the issuance of amendments, corrigenda, or errata. An official IEEE document at any point in time consists of the current edition of the document together with any amendments, corrigenda, or errata then in effect.

Every IEEE standard is subjected to review at least every ten years. When a document is more than ten years old and has not undergone a revision process, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE standard.

In order to determine whether a given document is the current edition and whether it has been amended through the issuance of amendments, corrigenda, or errata, visit the IEEE-SA Website at http://standards.ieee.org or contact IEEE at the address listed previously. For more information about the IEEE-SA or IEEE's standards development process, visit the IEEE-SA Website at http://standards.ieee.org.

Errata

Errata, if any, for all IEEE standards can be accessed on the IEEE-SA Website at the following URL: http://standards.ieee.org/findstds/errata/index.html. Users are encouraged to check this URL for errata periodically.

Patents

Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken by the IEEE with respect to the existence or validity of any patent rights in connection therewith. If a patent holder or patent applicant has filed a statement of assurance via an Accepted Letter of Assurance, then the statement is listed on the IEEE-SA Website at http://standards.ieee.org/about/sasb/patcom/patents.html. Letters of Assurance may indicate whether the Submitter is willing or unwilling to grant licenses under patent rights without compensation or under reasonable rates, with reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to obtain such licenses.

Essential Patent Claims may exist for which a Letter of Assurance has not been received. The IEEE is not responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patents Claims, or determining whether any licensing terms or conditions provided in connection with submission of a Letter of Assurance, if any, or in any licensing agreements are reasonable or non-discriminatory. Users of this standard are expressly advised that determination of the validity of any patent rights, and the risk of infringement of such rights, is entirely their own responsibility. Further information may be obtained from the IEEE Standards Association.

Participants

The following individuals were officers and members of the IEEE 802.3 Working Group at the beginning of the IEEE P802.3bu Working Group ballot. Individuals may have not voted, voted for approval, disapproval, or abstained on this amendment.

David J. Law, *IEEE 802.3 Working Group Chair*
Adam Healey, *IEEE 802.3 Working Group Vice-Chair*
Pete Anslow, *IEEE 802.3 Working Group Secretary*
Steven B. Carlson, *IEEE 802.3 Working Group Executive Secretary*
Valerie Maguire, *IEEE 802.3 Working Group Treasurer*

Dave Dwelley, *IEEE P802.3bu Power over Data Lines Task Force Chair, Phase 1*
Dan Dove, *IEEE P802.3bu Power over Data Lines Task Force Chair, Phase 2*
Andy Gardner, *IEEE P802.3bu Power over Data Lines Task Force Editor-in-Chief*
Craig Chabot, *IEEE P802.3bu Power over Data Lines Task Force PICS Editor*

David Abramson
Shadi Abughazaleh
Dale Amason
J. Michael Andrewartha
Eric Baden
Amrik Bains
Thananya Baldwin
Denis Beaudoin
Christian Beia
Michael Bennett
Vipul Bhatt
William Bliss
Brad Booth
Martin Bouda
Ralf-Peter Braun
Theodore Brillhart
Paul Brooks
Matthew Brown
Jairo Bustos Heredia
Adrian Butter
Juan-Carlos Calderon
J. Martin Carroll
Clark Carty
Geoffrey Chacon Simon
Mandeep Chadha
David Chalupsky
Jacky Chang
Xin Chang
Ahmad Chini
Keng Hua Chuang
Peter Cibula
Christopher R. Cole
Shaoan Dai
John D'Ambrosia
Yair Darshan
Piers Dawe
Wael Diab
Eric DiBiaso
Daniel Dillow
Chris Diminico
Thuyen Dinh
Curtis Donahue
Mike Dudek
Nick Duer
Frank Effenberger
Hesham Elbakoury
David Estes
John Ewen
Ramin Farjad
Shahar Feldman
German Feyh
Alan Flatman
Matthias Fritsche
Richard Frosch
Ali Ghiasi
Joel Goergen
Steven Gorshe
James Graba
Robert Grow
Mark Gustlin
Marek Hajduczenia
Bernie Hammond
Takehiro Hayashi
Yasuo Hidaka
Brian Holden
Rita Horner
Bernd Horrmeyer
Victor Hou
Yasuhiro Hyakutake
Hideki Isono
Tom Issenhuth
Kenneth Jackson
Andrew Jimenez
Chad Jones
Peter Jones
Manabu Kagami
Upen Kareti
Keisuke Kawahara
Yasuaki Kawatsu
Michael Kelsen
Yong Kim
Jonathan King
Scott Kipp
Michael Klempa
Shigeru Kobayashi
Keisuke Kojima
Paul Kolesar
Tom Kolze
Glen Kramer
Hans Lackner
Jeffrey Lapak
Mark Laubach
David Lewis
Jon Lewis
William Lo
Miklos Lukacs
Kent Lusted
Jeffery Maki
David Malicoat
James Malkemus
Yonatan Malkiman
Arthur Marris
Takeo Masuda
Kirsten Matheus
Erdem Matoglu
Laurence Matola
Brett McClellan
Thomas McDermott
John McDonough
Richard Mei
Richard Mellitz
Bryan Moffitt
Ardeshir Mohammadian
Leo Montreuil
Paul Mooney
Dale Murray
Henry Muyshondt
Edward Nakamoto
Gary Nicholl
Paul Nikolich
Kevin Noll
Mark Nowell
David Ofelt
Tom Palkert

Hui Pan
Sesha Panguluri
Carlos Pardo
Petar Pepeljugoski
Gerald Pepper
Ruben Perez-Aranda
Michael Peters
Rick Pimpinella
William Powell
Richard Prodan
Rick Rabinovich
Adee Ran
Alon Regev
Duane Remein
Victor Renteria
Martin Rossbach
Christopher Roth
Salvatore Rotolo
Vineet Salunke
Sam Sambasivan
Edward Sayre
Dieter Schicketanz
Fred Schindler
Peter Scruton
Hossein Sedarat
Naoshi Serizawa
Megha Shanbhag
Stephen Shellhammer
Ramin Shirani
Tom Skaar
Jeff Slavick
Scott Sommers
Tom Souvignier
Edward Sprague
Peter Stassar
Robert Stone
Junqing Sun
Steve Swanson
Andre Szczepanek
William Szeto
Bharat Tailor
Akio Tajima
Takayuki Tajima
Satoshi Takahashi
Kohichi Tamura
Alexander Tan
Mehmet Tazebay
Brian Teipen
Geoffrey Thompson
Pirooz Tooyserkani
Albert Tretter
Stephen Trowbridge
Yoshihiro Tsukamoto
Mike Tu
Sterling A. Vaden
Stefano Valle
Paul Vanderlaan
Robert Wagner
Roy Wang
Xinyuan Wang
Matthias Wendt
Oded Wertheim
Martin White
Natalie Wienckowski
Ludwig Winkel
Peter Wu
Yu Xu
Jun Yi
Lennart Yseboodt
Ting-Pa Yu
Hayato Yuki
Andrew Zambell
Yan Zhuang
George Zimmerman
Helge Zinner

The following members of the individual balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

David Abramson
Shadi Abughazaleh
Iwan Adhicandra
Thomas Alexander
Dale Amason
Pete Anslow
Stefan Aust
Amrik Bains
Charles Barest
Christian Boiger
Ralf-Peter Braun
Nancy Bravin
Jairo Bustos Heredia
William Byrd
Steven B. Carlson
Juan Carreon
Mandeep Chadha
Keith Chow
Keng Hua Chuang
Charles Cook
Rodney Cummings
Daniel Dove
Sourav Dutta
Richard Edgar
German Feyh
Norman Finn
Matthias Fritsche
Yukihiro Fujimoto
Andy Gardner
Devon Gayle
James Gilb
Joel Goergen
Randall Groves
Craig Gunther
Marco Hernandez
Guido Hiertz
Werner Hoelzl
Rita Horner
Noriyuki Ikeuchi
Osamu Ishida
Atsushi Ito
Raj Jain
Piotr Karocki
Stuart Kerry
Yongbum Kim
Bruce Kraemer
David J. Law
Jon Lewis
Arthur H. Light
William Lumpkins
Elvis Maculuba
Jeffery Maki
Arthur Marris
Michael Maytum
Edward McCall
Mick McCarthy
Brett McClellan
Thomas Mcdermott
Richard Mellitz
Tremont Miao
Jeffrey Moore
Charles Moorwood
Rick Murphy
Michael Newman
Nick S. A. Nikjoo
Paul Nikolich
Satoshi Obara
Bansi Patel
Arumugam Paventhan
Ruben Perez-Aranda
Michael Peters
Rick Pimpinella
Alon Regev
Maximilian Riegel
Robert Robinson
Benjamin Rolfe
Dan Romascanu
Frank Schewe
Dieter Schicketanz
Stefan Schneele
Thomas Starai
David Stover
Walter Struppler
Mitsutoshi Sugawara
Junqing Sun
Geoffrey Thompson
Mark-Rene Uchida
Sterling Vaden
Paul Vanderlaan
George Vlantis
Stephen Webb
Ludwig Winkel
Dayin Xu
Oren Yuen
Zhen Zhou
George Zimmerman

When the IEEE-SA Standards Board approved this standard on 7 December 2016, it had the following membership:

Jean-Philippe Faure, *Chair*
Ted Burse, *Vice Chair*
John D. Kulick, *Past Chair*
Konstantinos Karachalios, *Secretary*

Chuck Adams
Masayuki Ariyoshi
Stephen Dukes
Jianbin Fan
J. Travis Griffith
Gary Hoffman
Ronald W. Hotchkiss
Michael Janezic
Joseph L. Koepfinger*
Hung Ling
Kevin Lu
Annette D. Reilly
Gary Robinson
Mehmet Ulema
Yingli Wen
Howard Wolfman
Don Wright
Yu Yuan
Daidi Zhong

*Member Emeritus

Introduction

This introduction is not part of IEEE Std 802.3bu-2016, IEEE Standard for Ethernet—Amendment 8: Physical Layer and Management Parameters for Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the date of IEEE Std 802.3bu-2016 publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber

access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bp-2016

Amendment 4—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 97 and Clause 98. This amendment adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable in automotive and other applications not utilizing the structured wiring plant.

IEEE Std 802.3br-2016

Amendment 5—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 99. This amendment adds a MAC Merge sublayer and a MAC Merge Service Interface to support for Interspersing Express Traffic over a single link.

IEEE Std 802.3bn-2016

Amendment 6—This amendment adds the Physical Layer specifications and management parameters for symmetric and/or asymmetric operation of up to 10 Gb/s on point-to-multipoint Radio Frequency (RF) distribution plants comprising either amplified or passive coaxial media. It also extends the operation of Ethernet Passive Optical Networks (EPON) protocols, such as Multipoint Control Protocol (MPCP) and Operation Administration and Management (OAM).

IEEE Std 802.3bz-2016

Amendment 7—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 125 and Clause 126. This amendment adds new rates of 2.5 Gb/s and 5 Gb/s and new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bu-2016

Amendment 8—This amendment includes changes to IEEE Std 802.3-2015 to define a methodology for the provision of power via a single twisted pair to connected Data Terminal Equipment (DTE) with IEEE 802.3 single twisted-pair interfaces.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Contents

IEEE Standard for Ethernet

Amendment 8: Physical Layer and Management Parameters for Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.[1]

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

[1]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.4 Definitions

Insert the following definitions after 1.4.330 "Physical Signaling Sublayer (PLS)" as follows:

1.4.330a PoDL PD: A Powered Device that is intended to receive power from a link section consisting of a single twisted pair. (See IEEE Std 802.3, Clause 104.)

1.4.330b PoDL PSE: A device that provides power to a PoDL PD, connected via a link section consisting of a single twisted pair. DTE powering is intended to provide a single 100BASE-T1 or 1000BASE-T1 device with a unified interface for both the reception and transmission of data as well as the power to operate. (See IEEE Std 802.3, Clause 104.)

1.4.330c PoDL Regulated PSE: A PoDL PSE that is required to regulate the dc voltage at the PSE MDI/PI over the required range of PD load current.

1.4.330d PoDL Unregulated PSE: A PoDL PSE that is not required to regulate the voltage at the PSE MDI/PI over the required range of PD load current.

Change 1.4.338 as follows:

1.4.338 Power Sourcing Equipment (PSE): A DTE or midspan device that provides the power to a single link section. PSEs are defined for use with two different types of balanced twisted-pair PHYs. When used with 2 or 4 pair balanced twisted-pair (BASE-T) PHYs, (see IEEE Std 802.3, Clause 33), DTE powering is intended to provide a single 10BASE-T, 100BASE-TX, or 1000BASE-T device with a unified interface for both the data it requires and the power to process these data. When used with single balanced twisted-pair (BASE-T1) PHYs (see IEEE Std 802.3, Clause 104), DTE powering is intended to provide a single 100BASE-T1 or 1000BASE-T1 device with a unified interface for both the data it requires and the power to process these data. A PSE used with balanced single twisted-pair PHYs is also referred to as a PoDL PSE.

Change 1.4.415 as follows:

1.4.415 Type 1 PD: A PD that ~~does not provide a Class 4~~ provides a Class 0, 1, 2, or 3 signature during Physical Layer classification, and that is not a PoDL PD. (See IEEE Std 802.3, Clause 33.)

Insert the following definitions after 1.4.418 "Type 2 PSE" as follows:

1.4.418a Type A PoDL System: A system comprising a PoDL PSE, link section, and PD that are compatible with 100BASE-T1 PHYs.

1.4.418b Type B PoDL System: A system comprising a PoDL PSE, link section, and PD that are compatible with 1000BASE-T1 PHYs.

1.4.418c Type C PoDL System: A PoDL PSE, link section, and PD that are compatible with both 100BASE-T1 and 1000BASE-T1 PHYs.

1.4.418d Type D PoDL System: A PoDL PSE, link section, and PD that lack a data entity or are incompatible with IEEE 802.3 PHYs.

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphabetical order:

MFVS	Maintain Full Voltage Signature
PoDL	Power over Data Lines
SCCP	Serial Communication Classification Protocol

30. Management

Change the first paragraph of Clause 30 as follows:

This clause provides the Layer Management specification for DTEs, repeaters, MAUs, and Midspans based on the CSMA/CD access method. The clause is produced from the ISO framework additions to Clause 5, Layer Management; Clause 19, Repeater Management; and Clause 20, MAU Management. It incorporates additions to the objects, attributes, and behaviours to support 100 Mb/s, 1000 Mb/s and 10 Gb/s, full duplex operation, MAC Control, Link Aggregation, DTE Power via MDI, Power over Data Lines, subscriber access networks, and the Link Layer Discovery Protocol (LLDP) IEEE 802.3 Organizationally Specific TLVs. The objects, attributes, and behaviours to support Link Aggregation are deprecated by IEEE Std 802.1AX-2008.

30.2 Managed objects

30.2.2 Overview of managed objects

30.2.2.1 Text description of managed objects

Change the entry for oPHYEntity as follows:

oPHYEntity — If oOMPEmulation is implemented, oPHYEntity is contained within oOMPEmulation. Otherwise oPHYEntity is contained within oMACEntity. Many instances of oPHYEntity may coexist within one instance of oMACEntity; however, only one PHY may be active for data transfer to and from the MAC at any one time. oPHYEntity is the managed object that contains the MAU, PAF, ~~and~~ PSE, and PoDLPSE managed objects in a DTE.

Insert the following new entry for oPoDLPSE into the list, in alphabetical order:

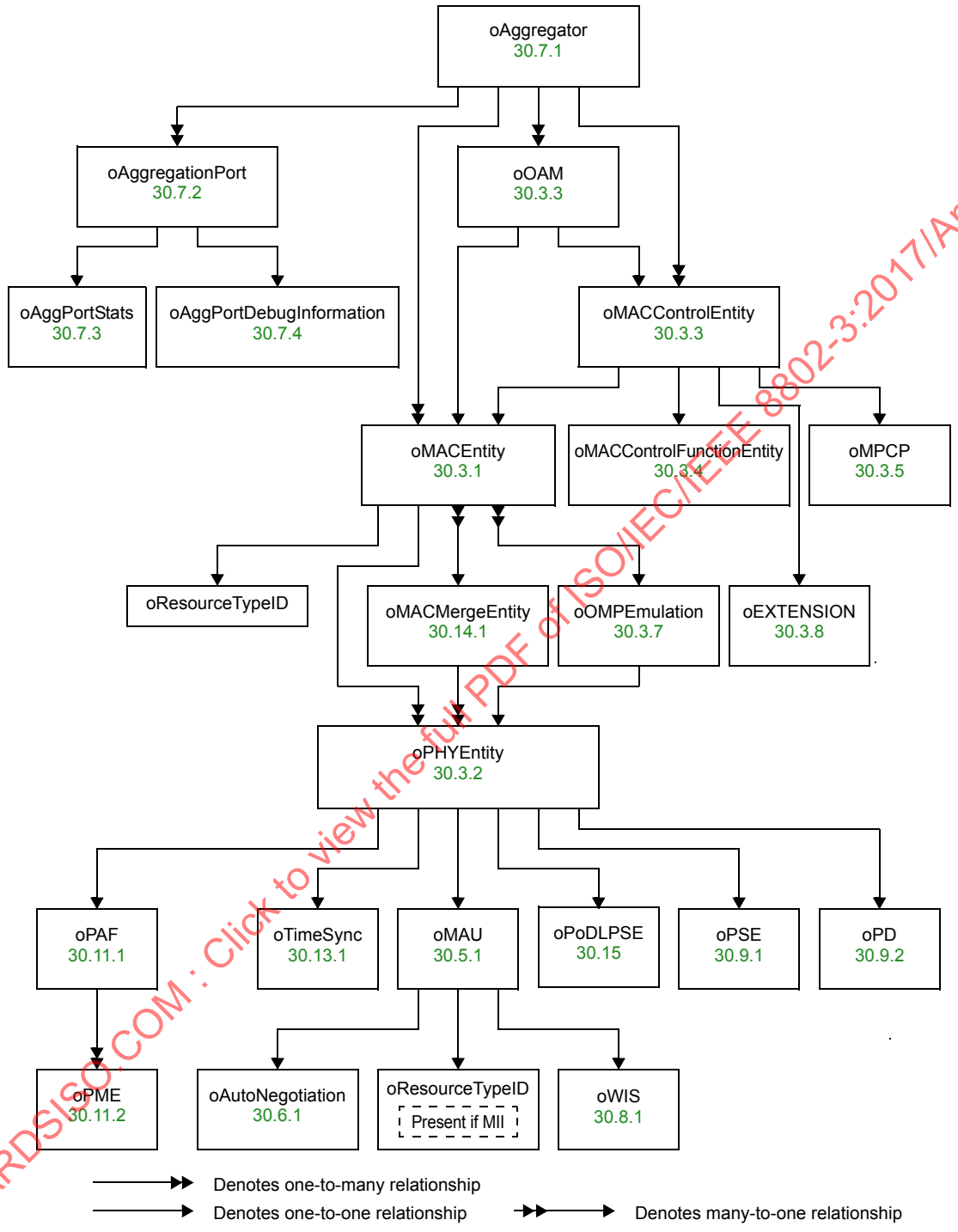
oPoDLPSE — The managed object of that portion of the containment trees shown in Figure 30–3. The attributes, notifications, and actions defined in 30.15 are contained within the PoDLPSE managed object.

30.2.3 Containment

Change the first paragraph of 30.2.3 as follows:

A containment relationship is a structuring relationship for managed objects in which the existence of a managed object is dependent on the existence of a containing managed object. The contained managed object is said to be the subordinate managed object, and the containing managed object the superior managed object. The containment relationship is used for naming managed objects. The local containment relationships among object classes are depicted in the entity relationship diagrams, Figure 30–3 through Figure 30–6. These figures show the names of the object classes and whether a particular containment relationship is one-to-one, one-to-many or many-to-one. For further requirements on this topic, see IEEE Std 802.1F-1993. PSE and PoDL PSE management are ~~is~~ only valid in a system that provides management at the next higher containment level, that is, either a DTE, or in the case of PSE management only, a repeater or Midspan with management.

Replace Figure 30-3 (as modified by IEEE Std 802.3br-2016) with the following:



Note—The objects oAggregator, oAggregationPort, oAggPortStats and oAggPortDebugInformation are deprecated by IEEE Std 802.1AX-2008.

Figure 30–3— DTE System entity relationship diagram

30.2.5 Capabilities

Change the first paragraph in 30.2.5 as follows:

This standard makes use of the concept of packages as defined in ISO/IEC 10165-4:1992 as a means of grouping behaviour, attributes, actions, and notifications within a managed object class definition. Packages may either be mandatory, or be conditional, that is to say, present if a given condition is true. Within this standard capabilities are defined, each of which corresponds to a set of packages, which are components of a number of managed object class definitions and which share the same condition for presence. Implementation of the appropriate Basic and Mandatory packages is the minimum requirement for claiming conformance to IEEE 802.3 Management. Implementation of an entire optional capability is required in order to claim conformance to that capability. The capabilities and packages for IEEE 802.3 Management are specified in Table 30–1a through ~~Table 30–9~~ Table 30–10.

Change the ninth paragraph as follows:

For managed PSEs, the PSE Basic Package is mandatory and the PSE Recommended Package is optional. For managed PoDL PSEs, the PoDLPSE Basic Package is mandatory and the PoDLPSE Recommended Package is optional. For managed PDs, the PD Basic Package is mandatory. For a managed PSE to be conformant to this standard, it shall fully implement the PSE Basic Package. For a managed PoDL PSE to be conformant to this standard, it shall fully implement the PoDLPSE Basic Package. For a managed PD to be conformant to this standard, it shall fully implement the PD Basic Package. For a managed PSE to be conformant to the optional Recommended Package it shall implement that entire package. For a managed PoDL PSE to be conformant to the optional PoDL PSE Recommended Package it shall implement that entire package. PSE, ~~and~~ PD, PoDL PSE, and PoDL PD management is optional with respect to all other CSMA/CD management.

Insert new Table 30-10 as follows:

Table 30–10—PoDL PSE capabilities

			PoDLPSE Basic Package (mandatory)	PoDLPSE Recommended Package (optional)
oResourceTypeID managed object				
aResourceTypeIDName	ATTRIBUTE	GET	X	
aResourceInfo	ATTRIBUTE	GET	X	
oPoDLPSE managed object class (30.15)				
aPoDLPSEID	ATTRIBUTE	GET	X	
aPoDLPSEAdminState	ATTRIBUTE	GET	X	
aPoDLPSEPowerDetectionStatus	ATTRIBUTE	GET	X	
aPoDLPSEType	ATTRIBUTE	GET	X	
aPoDLPSEDetectedPDType	ATTRIBUTE	GET	X	
aPoDLPSEDetectedPDPowerClass	ATTRIBUTE	GET	X	
aPoDLPSEInvalidSignatureCounter	ATTRIBUTE	GET		X
aPoDLPSEInvalidClassCounter	ATTRIBUTE	GET		X
aPoDLPSEPowerDeniedCounter	ATTRIBUTE	GET		X
aPoDLPSEOverLoadCounter	ATTRIBUTE	GET		X
aPoDLPSEMaintainFullVoltageSignatureAbsentCounter	ATTRIBUTE	GET		X
aPoDLPSEActualPower	ATTRIBUTE	GET		X
aPoDLPSEPowerAccuracy	ATTRIBUTE	GET		X
aPoDLPSECumulativeEnergy	ATTRIBUTE	GET		X
acPoDLPSEAdminControl	ACTION		X	
Common Attributes Template				
aCMCounter	ATTRIBUTE	GET		X

Insert 30.15 after 30.14 (as inserted by IEEE Std 802.3br-2016) as follows:

30.15 Layer management for Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet

30.15.1 PoDL PSE managed object class

This subclause formally defines the behaviours for the oPoDLPSE managed object class attributes and actions.

30.15.1.1 PoDL PSE attributes

30.15.1.1.1 aPoDLPSEID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aPoDLPSEID is assigned so as to uniquely identify a PoDL PSE among the subordinate managed objects of the containing object.;

30.15.1.1.2 aPoDLPSEAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

enabled	PoDL PSE functions enabled
disabled	PoDL PSE functions disabled

BEHAVIOUR DEFINED AS:

A read-only value that identifies the operational state of the PoDL PSE functions. An interface that can provide the PoDL PSE functions specified in Clause 104 is enabled to do so when this attribute has the enumeration "enabled." When this attribute has the enumeration "disabled" the interface acts as if it had no PoDL PSE function. The operational state of the PSE function can be changed using the acPoDLPSEAdminControl action.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PSE Enable bit specified in 45.2.7b.1.2.;

30.15.1.1.3 aPoDLPSEPowerDetectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	true state unknown
disabled	PoDL PSE disabled
searching	PoDL PSE searching
deliveringPower	PoDL PSE delivering power
sleep	PoDL PSE sleep
idle	PoDL PSE idle
error	PoDL PSE error

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PoDL PSE.

The enumeration "disabled" is asserted true when the PoDL PSE state diagram variable mr_pse_enable is false (see 104.4.3.3). The enumeration "deliveringPower" is asserted true when the PoDL PSE state diagram variable pi_powered is true. The enumeration "sleep" is asserted true when the PoDL PSE state diagram variable pi_sleeping is true. The enumeration "searching" is asserted true when either of the PSE state diagram variables pi_detecting or pi_classifying is true. The enumeration "idle" is asserted true when the logical combination of the PoDL PSE state diagram variables pi_prebiased*!pi_sleeping

is true. The enumeration “error” is asserted true when the PoDL PSE state diagram variable overload_held is true.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PSE Status bits specified in 45.2.7b.2.9.;

30.15.1.1.4 aPoDLPSEType

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	initializing, true state not yet known
typeA	Type A PoDL PSE
typeB	Type B PoDL PSE
typeC	Type C PoDL PSE
typeD	Type D PoDL PSE

BEHAVIOUR DEFINED AS:

A read-only value that identifies the PoDL PSE Type specified in 104.4.1.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PSE Type bits specified in 45.2.7b.2.7.;

30.15.1.1.5 aPoDLPSEDetectedPDType

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	initializing, true state not yet known
typeA	Type A PoDL PD
typeB	Type B PoDL PD
typeC	Type C PoDL PD
typeD	Type D PoDL PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the Type of the detected PoDL PD as specified in 104.5.1. This value is only valid while a PD is being powered, that is the attribute aPoDLPSEPowerDetectionStatus is reporting the enumeration “deliveringPower”.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PD Type bits specified in 45.2.7b.3.2.;

30.15.1.1.6 aPoDLPSEDetectedPDPowerClass

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	initializing, true state not yet known
class0	Class 0 PoDL PD
class1	Class 1 PoDL PD
class2	Class 2 PoDL PD
class3	Class 3 PoDL PD

class4	Class 4 PoDL PD
class5	Class 5 PoDL PD
class6	Class 6 PoDL PD
class7	Class 7 PoDL PD
class8	Class 8 PoDL PD
class9	Class 9 PoDL PD

BEHAVIOUR DEFINED AS:

A read-only value that indicates the class of the detected PoDL PD as specified in Table 104–1. This value is only valid while a PD is being powered, that is the attribute aPoDLPSEPowerDetectionStatus is reporting the enumeration “deliveringPower”.

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the PD Class bits specified in 45.2.7b.2.8.;

30.15.1.1.7 aPoDLPSEInvalidSignatureCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram variable mr_invalid_signature transitions from false to true (see 104.4.3.3).

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the invalid signature bit specified in 45.2.7b.2.3.;

30.15.1.1.8 aPoDLPSEInvalidClassCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram variable tclass_timer_done transitions from false to true or when the valid_class variable transitions from true to false (see 104.4.3.3).

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the class timeout bit specified in 45.2.7b.2.4.;

30.15.1.1.9 aPoDLPSEPowerDeniedCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PoDL PSE state diagram variable power_available transitions from true to false (see 104.4.3.3).

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the power denied bit specified in 45.2.7b.2.1.;

30.15.1.1.10 aPoDLPSEOverLoadCounter

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 13 counts per 10 seconds.

BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram variable overload_held transitions from false to true (see 104.4.3.3).

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the overload bit specified in 45.2.7b.2.5.;

30.15.1.1.11 aPoDLPSEMaintainFullVoltageSignatureAbsentCounter

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 33 counts per 10 seconds.

BEHAVIOUR DEFINED AS:
This counter is incremented when the PoDL PSE state diagram variable mfvs_timeout transitions from false to true (see 104.4.3.3).

If a Clause 45 MDIO Interface to the PoDL PSE function is present, then this attribute may be derived from the Maintain Full Voltage Signature Absent bit specified in 45.2.7b.2.6.;

30.15.1.1.12 aPoDLPSEActualPower

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
An integer value indicating present (actual) power being supplied by the PoDL PSE as measured at the MDI in milliwatts. The behaviour is undefined if the state of aPoDLPSEPowerDetectionStatus is anything other than “deliveringPower”. The sampling frequency and averaging are vendor-defined.;

30.15.1.1.13 aPoDLPSEPowerAccuracy

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A signed integer value indicating the accuracy associated with aPoDLPSEActualPower in milliwatts.;

30.15.1.1.14 aPoDLPSECumulativeEnergy

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. The counter has a maximum increment rate of 100,000 per second.

BEHAVIOUR DEFINED AS:

A count of the cumulative energy supplied by the PoDL PSE, measured at the MDI, and expressed in units of millijoules.;

30.15.1.2 PoDL PSE actions

30.15.1.2.1 acPoDLPSEAdminControl

ACTION

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

enabled	PoDL PSE functions enabled
disabled	PoDL PSE functions disabled

BEHAVIOUR DEFINED AS:

This action provides a means to alter aPoDLPSEAdminState.;

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

Insert row to add Power Unit Registers to Table 45-1 (as modified by IEEE Std 802.3bn-2016) directly above reserved row, and adjust reserved row as follows (unchanged rows not shown):

Table 45–1—MDIO Manageable Device addresses

Device address	MMD name
13	Power Unit
14~~13~~ through 28	Reserved

Change Table 45-2 (as modified by IEEE Std 802.3bn-2016) to update reserved row and insert row to add Power Unit Registers in Table 45-2, below reserved row for m.5.15:13 and immediately above row for register m.5.12 (inserted by IEEE Std 802.3bn-2016) (unchanged rows not shown):

Table 45–2—Devices in package registers bit definitions

Bit(s)[a]	Name	Description	R/W[b]
m.5.15:~~13~~ 14	Reserved	Value always 0	RO
m.5.13	Power Unit present	1 = Power Unit present in package 0 = Power Unit not present in package	RO

[a]m = address of MMD accessed (see Table 45–1)
[b]RO = Read only

Insert the following subclauses for Power Unit Registers immediately after 45.2.7a.6 (10GPASS-XR receive MER measurement registers) added by IEEE Std 802.3bn-2016.

45.2.7b Power Unit Registers

The assignment of registers in the Power Unit MMD is shown in Table 45–211p.

Table 45–211p—Power Unit MMD Registers

Register address	Register name	Subclause
13.0	PoDL PSE Control	45.2.7b.1
13.1	PoDL PSE Status 1	45.2.7b.2
13.2	PoDL PSE Status 2	45.2.7b.3

45.2.7b.1 PoDL PSE Control register (Register 13.0)

The assignment of bits in the PoDL PSE Control register is shown in Table 45–211q. The default value for each bit of the PoDL PSE Control register should be chosen so that the initial state of the PSE upon power up or reset is a normal operational state without management intervention.

Table 45–211q—PoDL PSE Control register bit definitions

Bit(s)	Name	Description	R/W[a]
13.0.15:2	Reserved	Value always 0	RO
13.0.1	Enable power classificatioin	1 = Power classification enabled 0 = Power classification disabled	R/W
13.0.0	PSE Enable	1 = PSE Enabled 0 = PSE Disabled	R/W

[a]R/W = Read/Write, RO = Read Only

45.2.7b.1.1 Enable power classification (13.0.1)

The power classification function is enabled by setting bit 13.0.1 to one and disabled by setting bit 13.0.1 to zero. This bit maps to the mr_sccp_enabled variable (see 104.4.3.3).

45.2.7b.1.2 PSE Enable (13.0.0)

When bit 13.0.0 is set to zero, the PSE function shall be disabled. When bit 13.0.0 is set to one, the PSE function shall be enabled. This register bit maps to the mr_pse_enable variable (see 104.4.3.3).

45.2.7b.2 PoDL PSE Status 1 register (Register 13.1)

The assignment of bits in the PoDL PSE Status 1 register is shown in Table 45–211r.

Table 45–211r—PoDL PSE Status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
13.1.15	Power Denied	1 = Power has been denied due to power not available 0 = Power has not been denied due to power not available	RO/ LH
13.1.14	Valid Signature	1 = Valid PD signature detected 0 = No valid PD signature detected	RO/ LH
13.1.13	Invalid Signature	1 = Invalid PD signature detected 0 = No invalid PD signature detected	RO/ LH
13.1.12	Class Timeout	1 = Classification timeout condition detected 0 = No Classification timeout condition detected	RO/ LH
13.1.11	Overload	1 = Overload condition detected 0 = No overload condition detected	RO/ LH
13.1.10	MFVS Absent	1 = MFVS absent condition detected 0 = No MFVS absent condition detected	RO/ LH
13.1.9:7	PSE Type	9 8 7 1 x x = Reserved 0 1 1 = Type D PSE 0 1 0 = Type C PSE 0 0 1 = Type B PSE 0 0 0 = Type A PSE	RO
13.1.6:3	PD Class	6 5 4 3 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = Class code 9 1 0 0 0 = Class code 8 0 1 1 1 = Class code 7 0 1 1 0 = Class code 6 0 1 0 1 = Class code 5 0 1 0 0 = Class code 4 0 0 1 1 = Class code 3 0 0 1 0 = Class code 2 0 0 0 1 = Class code 1 0 0 0 0 = Class code 0	RO
13.1.2:0	PSE Status	2 1 0 1 1 1 = Unknown 1 1 0 = Reserved 1 0 1 = Idle 1 0 0 = Error 0 1 1 = Searching 0 1 0 = Delivering power 0 0 1 = Sleep 0 0 0 = Disabled	RO

[a]RO = Read Only, LH = Latching High

45.2.7b.2.1 Power Denied (13.1.15)

When read as a one, bit 13.1.15 indicates that application of full operating voltage at the PI has been denied. This bit shall be set to one when power_available transitions from true to false (see 104.4.3.3). The Power Denied bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.2 Valid Signature (13.1.14)

When read as a one, bit 13.1.14 indicates that a valid signature has been detected. This bit shall be set to one when mr_valid_signature transitions from false to true (see 104.4.3.3). The Valid Signature bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.3 Invalid Signature (13.1.13)

When read as a one, bit 13.1.13 indicates that an invalid signature has been detected. This bit maps to the PSE state diagram variable mr_invalid_signature, and latches high when mr_invalid_signature transitions from false to true (see 104.4.3.3). The Invalid Signature bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.4 Class Timeout (13.1.12)

When read as a one, bit 13.1.12 indicates that a Classification timeout condition has been detected. The Class Timeout bit shall be set to one when tclass_timer_done transitions from false to true (see 104.4.3.3). The Class Timeout bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.5 Overload (13.1.11)

When read as a one, bit 13.1.11 indicates that an overload condition has been detected. This bit shall be set to one when the PSE state diagram variable overload_held transitions from false to true (see 104.4.3.3). The Overload bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.6 MFVS Absent (13.1.10)

When read as a one, bit 13.1.10 indicates that an MFVS Absent condition has been detected. The MFVS Absent bit shall be set to one when mfvs_timeout transitions from false to true (see 104.4.3.3). The MFVS Absent bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.2.7 PSE Type (13.1.9:7)

Bits 13.1.9:7 report the PSE Type of the PSE as specified in 104.4.1. When read as 000, bits 13.1.9:7 indicate a Type A PSE, when read as 001 a Type B PSE is indicated, and when read as 010 a Type C PSE is indicated. and when read as 011 a Type D PSE is indicated. Values of 1xx are reserved.

45.2.7b.2.8 PD Class (13.1.6:3)

Bits 13.1.6:3 report the PD Class of a detected PD as specified in 104.5.2. The value in this register is valid while a PD is connected, i.e., while the PSE Status (13.1.2:0) bits are reporting “delivering power”. When read as 0000 a Class 0 PD is indicated, when read as 0001 a Class 1 PD is indicated, when read as 0010 a Class 2 PD is indicated, when read as 0011 a Class 3 PD is indicated, when read as 0100 a Class 4 PD is indicated, when read as 0101 a Class 5 PD is indicated, when read as 0110 a Class 6 PD is indicated, when read as 0111 a Class 7 PD is indicated, when read as 1000 a Class 8 PD is indicated, and when read as 1001 a Class 9 PD is indicated.

45.2.7b.2.9 PSE Status (13.1.2:0)

Bits 13.1.2:0 report the current status of the PSE. When read as 000, bits 13.1.2:0 indicate that mr_pse_enable is asserted false (see 104.4.3.3). When read as 001, bits 13.1.2:0 indicate that pi_sleeping is asserted true. When read as 010, bits 13.1.2:0 indicate that pi_powered is asserted true. When read as 011, bits 13.1.2:0 indicate that either pi_detecting or pi_classifying is are asserted true. When read as 100, bits 13.1.2:0 indicate that overload_held is asserted true. When read as 101, bits 13.1.2:0 indicate that the logical

combination pi_prebiased*!pi_sleeping is true. When read as 111, bits 13.1.2:0 indicate that the PSE status is unkown. Bit combination 110 is reserved.

45.2.7b.3 PoDL PSE Status 2 register (Register 13.2)

The PoDL PSE Status 2 register is an extension of the PoDL PSE Status 1 register. Assignment of bits in the PoDL PSE Status 2 register is shown in Table 45–211s.

Table 45–211s—PoDL PSE Status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
13.2.15	Invalid Class	1 = Invalid PD class detected 0 = No invalid PD class detected	RO/LH
13.2.14:3	Reserved	Value always 0	RO
13.2.2:0	PD Type	2 1 0 1 1 1 = Unknown 1 1 0 = Reserved 1 0 x = Reserved 0 1 1 = Type D PD 0 1 0 = Type C PD 0 0 1 = Type B PD 0 0 0 = Type A PD	RO

[a]RO = Read Only, LH = Latching High

45.2.7b.3.1 Invalid Class (13.2.15)

When read as a one, bit 13.2.15 indicates that an invalid class has been detected. This bit maps to the PSE state diagram variable valid_class, and latches high when do_classification_done is true and valid_class is false (see 104.4.3.3). The Invalid Class bit shall be implemented with latching high behavior as defined in 45.2.

45.2.7b.3.2 PD Type (13.2.2:0)

Bits 13.2.2:0 report a value of 111 until a valid classification has taken place, or if no PD is present. A value of 111 indicates that the PSE has not performed classification and therefore cannot indicate the proper value for the PD Type. Once a valid classification has occurred, the value of these bits reflect the PD Type of an attached PD as specified in 104.5.1. When read as 000, bits 13.2.2:0 indicate a Type A PD; when read as 001, a Type B PD is indicated; when read as 010, a Type C PD is indicated; and when read as 011, a Type D PD is indicated. Values of 10x and 110 are reserved.

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, MDIO interface

45.5.3 Major capabilities/options

Insert the following row at the bottom of the Major capabilities/options table

Item	Feature	Subclause	Value/Comment	Status	Support
*PODL	Implementation of Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet	45.2.7b		O	Yes [ ] No [ ] N/A[ ]

45.5.3.13b Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet management functions

Insert 45.5.3.13b after 45.5.3.13a (inserted by IEEE Std 802.3bn-2016) as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
PODLM1	PSE Enable bit	45.2.7b.1.2	PSE function enabled when set to one and disabled when set to zero	PODL: M	Yes [ ] N/A[ ]
PODLM2	Power Denied bit	45.2.7b.2.1	Implemented with latching high behavior and set to one when power_available transitions from true to false	PODL: M	Yes [ ] N/A[ ]
PODLM3	Valid Signature bit	45.2.7b.2.2	Implemented with latching high behavior and set to one when mr_valid_signature transitions from false to true	PODL: M	Yes [ ] N/A[ ]
PODLM4	Invalid Signature bit	45.2.7b.2.3	Implemented with latching high behavior and set to one when mr_valid_signature transitions from false to true	PODL: M	Yes [ ] N/A[ ]
PODLM5	Class Timeout bit	45.2.7b.2.4	Implemented with latching high behavior and set to one when tclass_timer_done transitions from false to true	PODL: M	Yes [ ] N/A[ ]
PODLM6	Overload bit	45.2.7b.2.5	Implemented with latching high behavior and set to one when overload_held transitions from false to true	PODL: M	Yes [ ] N/A[ ]
PODLM7	MFVS Absent bit	45.2.7b.2.6	Implemented with latching high behavior and set to one when mfvs_timeout transitions from false to true	PODL: M	Yes [ ] N/A[ ]
PODLM8	Invalid Class bit	45.2.7b.3.1	Implemented with latching high behavior as defined in 45.2	PODL: M	Yes [ ] N/A[ ]

96. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T1

96.5.4.1 Transmitter output droop

Add the following paragraph after the first paragraph of 96.5.4.1:

When a Clause 104 Type A or Type C PI is encompassed within the MDI, the magnitude of both the positive and negative droop measured with respect to an initial peak value after the zero crossing and the value 500 ns after the initial peak, shall be less than 60%.

96.8.2.1 MDI return loss

Add the following paragraph after the first paragraph of 96.8.2.1:

When a Clause 104 Type A or Type C PI is encompassed within the MDI, the MDI return loss (RL) shall meet or exceed Equation (96–11a) for all frequencies from 1 MHz to 66 MHz (with 100 Ω reference impedance) at all times when the PHY is transmitting data or control symbols.

Add the following formula as Equation (96-11a) after Equation (96-11):

$$\text{MDI return loss}(f) \geq \begin{cases} 20 - 20 \times \log_{10}\left(\frac{2}{f}\right) & 1 \leq f < 2 \\ 20 & 2 \leq f < 30 \\ 20 - 20 \times \log_{10}\left(\frac{f}{30}\right) & 30 \leq f < 66 \end{cases} \text{dB} \qquad (96\text{–}11a)$$

104. Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet

104.1 Overview

This clause defines the functional and electrical characteristics of two optional power entities, a PoDL Powered Device (PD) and PoDL Power Sourcing Equipment (PSE), for use with supported single balanced twisted-pair Ethernet Physical Layers. When used in this clause, the term PSE always means PoDL PSE, and the term PD always means PoDL PD. These entities allow devices to supply/draw power using the same cabling that may be used for data transmission. PoDL is intended to provide a single balanced twisted-pair Ethernet Physical Layer device with a single interface to both the data it requires and the power to process this data. This clause specifies the following:

a) The characteristics of a power source to add power to the 100 Ω single balanced twisted-pair cabling system.
b) The characteristics of a PD's load on the power source and the cabling.
c) Certain electrical parameters of each MDI/PI that may be different from that specified in the PHY clause when power is simultaneously transmitted with data.
d) Physical Layer protocols allowing the detection of a device that requests power from a PSE and classification of the device based on its power needs.
e) A method for Powered Devices and Power Sourcing Equipment to negotiate and allocate power.
f) A method for scaling supplied voltage back to the sleep level when full operating voltage is no longer requested or required.

This clause differentiates between the two ends of the link, defining the PSE and the PD as separate but related devices within a PoDL system.

104.1.1 Compatibility considerations

Compliant implementations of PD and PSE systems are defined as compatible at their respective Power Interfaces (PIs) when used in accordance with the restrictions of this clause. Designers are free to implement circuitry within the PD and PSE in an application-dependent manner provided that the respective PI specifications are satisfied. MDIs that incorporate compliant PoDL PIs are compatible with their respective Physical Layer standards. Such compatibility may require additional specifications found within this clause (see 104.6).

104.1.2 Relationship of PoDL to the IEEE 802.3 architecture

PoDL is an optional power entity to be used in conjunction with supported single-pair Ethernet Physical Layers. Data that is out of band to normal Ethernet traffic may be transmitted and received between the PSE and PD prior to the application of power and subsequent to the removal of full operating voltage via the MDI using the Serial Communication Classification Protocol (SCCP) which is described in 104.7.

Figure 104–1 depicts the positioning of PoDL for the PSE. Figure 104–2 depicts the positioning of PoDL in the case of the PD.

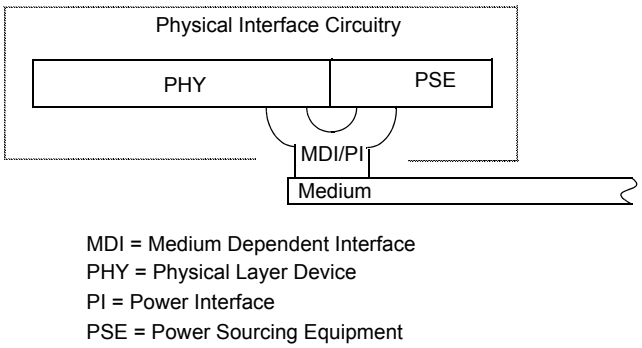


Figure 104–1—PoDL Power Sourcing Equipment (PSE) relationship to the physical interface circuitry and the IEEE 802.3 Ethernet model

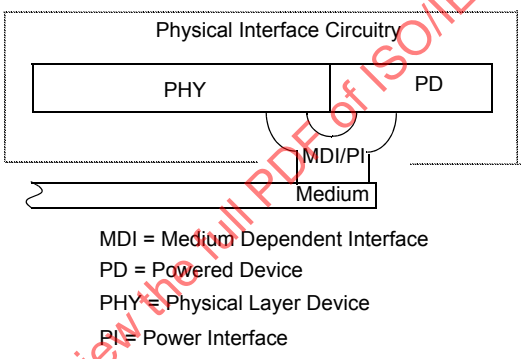


Figure 104–2—PoDL Powered Device (PD) relationship to the physical interface circuitry (PHY) and the IEEE 802.3 Ethernet model

The Power Interface (PI) is the generic term that refers to the mechanical and electrical interface between the PSE or PD and the transmission medium. The PI is encompassed within the MDI.

104.1.3 PoDL system types

A PoDL system consists of a PSE, a link segment, and a PD. A Type A or Type C PSE and Type A or Type C PD is compatible with 100BASE-T1 PHYs. A Type B or Type C PSE and Type B or Type C PD is compatible with 1000BASE-T1 PHYs. A Type C PSE and Type C PD is compatible with both 100BASE-T1 and 1000BASE-T1 PHYs. Type D PSEs and Type D PDs may be incompatible with IEEE 802.3 PHYs and may lack a data entity.

Figure 104–3 illustrates the block diagram for a PoDL system.

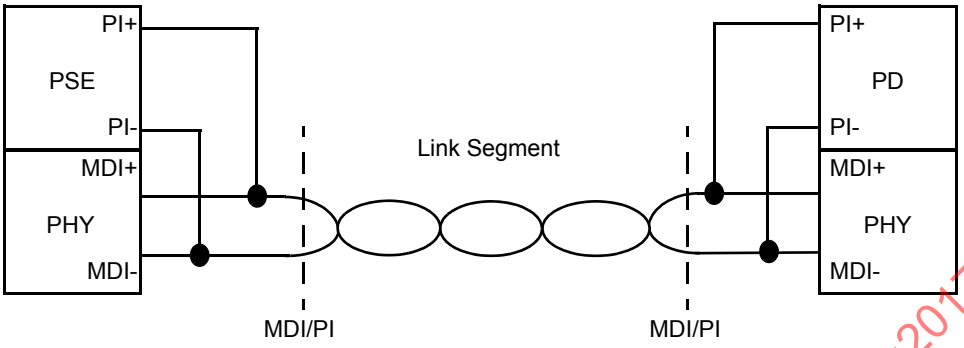


Figure 104–3—PoDL system block diagram

NOTE—PI elements that prevent loading of the data signal by the PSE and PD are not shown. PHY elements that block dc are not shown.

104.2 Link segment

The dc loop resistance of the link segment shall be less than 6 Ω for 12 V unregulated classes. The dc loop resistance shall be less than 6.5 Ω for 12 V regulated, 24 V regulated and unregulated, and 48 V regulated classes.

104.3 Class power requirements

PSEs and PDs are further categorized by their class. These classes and the relevant electrical specifications are shown in Table 104–1.

Table 104–1—Class power requirements matrix for PSE, PI, and PD

	12 V unregulated PSE		12 V regulated PSE		24 V unregulated PSE		24 V regulated PSE		48 V regulated PSE	
Class	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
$V_{PSE(max)}$ (V)[a]	18	18	18	18	36	36	36	36	60	60
$V_{PSE\_OC(min)}$ (V)[b]	6	6	14.4	14.4	12	12	26	26	48	48
$V_{PSE(min)}$ (V)	5.6	5.77	14.4	14.4	11.7	11.7	26	26	48	48
$I_{PI(max)}$ (mA)[c]	101	227	249	471	97	339	215	461	735	1 360
$P_{Class(min)}$ (W)[d]	0.566	1.31	3.59	6.79	1.14	3.97	5.59	12	35.3	65.3
$V_{PD(min)}$ (V)	4.94	4.41	12	10.6	10.3	8.86	23.3	21.7	40.8	36.7
$P_{PD(max)}$ (W)[e]	0.5	1	3	5	1	3	5	10	30	50

[a] $V_{PSE(max)}$ is the maximum allowed voltage at the PSE PI over the full range of operating conditions.
[b] $V_{PSE\_OC(min)}$ is the minimum allowed open circuit voltage measured at the PSE PI.
[c] $I_{PI(max)}$ is the maximum current flowing at the PSE and PD PIs except during inrush or an overload condition. $I_{PI(max)}$ may be exceeded during inrush or an overload (see 104.4.6.2). Users are cautioned to be aware of the ampacity of cabling, as installed, and local codes and regulations (see 104.8.1).
[d] $P_{Class(min)}$ is the minimum average available output power at the PSE PI.
[e] $P_{PD(max)}$ is the maximum average available power at the PD PI.

104.4 Power Sourcing Equipment (PSE)

The PSE provides power to the PD. The PSE's main functions are as follows:

a) To search the link segment for a PD
b) To supply power to a detected PD through the link segment
c) To monitor the power applied to a link segment
d) To remove the full operating voltage when no longer required, when transitioning to the SLEEP state, or when a short-circuit or other fault is detected

Voltage and power classification mechanisms exist via the Serial Communication Classification Protocol (SCCP) to provide the PSE with detailed information regarding the requirements of the PD and vice versa.

A PSE is specified by its electrical and logical behavior as seen at the PI.

104.4.1 PSE types

For PoDL systems there are multiple types of PSEs—Type A, Type B, Type C, and Type D consistent with 104.1.3.

104.4.2 PSE classes

A PSE shall comply with the voltage and power requirements listed in Table 104–1 for the relevant class.

104.4.3 PSE state diagram

The PSE shall implement the behavior of the state diagrams shown in Figure 104–4, Figure 104–5, and Figure 104–6.

104.4.3.1 Overview

Prior to application of full operating voltage at the PI, the PSE performs detection in order to verify that a valid PD is present. A PSE may apply full operating voltage if it is able to successfully classify the PD using SCCP.

After full operating voltage has been applied, the PSE monitors the PI for a valid Maintain Full Voltage Signature (MFVS) from the PD. In the event a valid MFVS is not present, the PSE reduces the voltage at the PI to the range of V_{Sleep}. If an external wakeup request is received or if a valid wakeup current signature is detected at the PI, the PSE confirms that a valid PD is present by re-performing detection and, if enabled, classification before reapplying full operating voltage to the PI.

Additionally, while voltage is applied, the PSE monitors the current drawn and removes power if it detects an overload, short-circuit, or other fault.

104.4.3.2 Conventions

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

104.4.3.3 Variables

The PSE state diagrams use the following variables:

detection_done
: TRUE: the detection sequence has terminated since the last entry to the IDLE state either as a result of a valid or invalid signature being detected.
FALSE: the detection sequence has not terminated since the last entry to the IDLE state either as a result of a valid or invalid signature being detected.

do_classification_done
: TRUE: following a detection sequence, the PSE has concluded serial communication after performing a read of the PD information and any additional implementation dependent read or write commands.
FALSE: following a detection sequence, the PSE has not concluded serial communication after performing a read of the PD information and any additional implementation dependent read or write commands.

external_wakeup
: TRUE: while in the SLEEP state, the PSE has received an external wakeup request.
FALSE: while in the SLEEP state, the PSE has not received an external wakeup request.

iprebias_valid
: TRUE: the PSE pre-bias output current is valid (see 104.4.6.2.3).
FALSE: the PSE pre-bias output current is invalid (see 104.4.6.2.3).

mfvs_timeout

TRUE: the MFVS dropout timer has timed out.
FALSE: the MFVS dropout timer has not timed out.

mfvs_valid
TRUE: MFVS is present (see 104.4.7.1).
FALSE: MFVS is absent (see 104.4.7.1).

mr_pse_enable
TRUE: enable operation of the PSE.
FALSE: disable operation of the PSE.

mr_sccp_enabled
TRUE: SCCP is enabled (see 104.7).
FALSE: SCCP is not enabled (see 104.7).

mr_invalid_signature
TRUE: an invalid signature has been detected during the detection cycle subsequent to the last idle sequence.
FALSE: an invalid signature has not been detected.

mr_valid_signature
TRUE: a valid PD signature has been detected during the detection cycle subsequent to the last idle sequence.
FALSE: a valid PD signature has not been detected.

overload_detected
TRUE: the PSE has detected an overload condition (see 104.4.6.2.1).
FALSE: the PSE has not detected an overload condition.

overload_held
TRUE: overload_detected has been TRUE since last entry to the IDLE state.
FALSE: overload_detected has been FALSE since last entry to the IDLE state.

pd_wakeup
TRUE: while in the SLEEP state, the PSE has detected a valid wakeup current signature.
FALSE: while in the SLEEP state, the PSE has not detected a valid wakeup current signature.

pi_classifying
TRUE: the PSE is performing classification at the PI (see 104.7).
FALSE: the PSE is not performing classification at the PI.

pi_detecting
TRUE: the circuitry that forces a voltage limited detection current and senses the voltage at the PI is enabled (see 104.4.4).
FALSE: the circuitry that forces a voltage limited detection current and senses the voltage at the PI is disabled.

pi_discharge_en
TRUE: the circuitry that discharges the PI to V_{Sleep} is enabled.
FALSE: the circuitry that discharges the PI to V_{Sleep} is disabled.

pi_powered
TRUE: the circuitry that applies full operating voltage to the PI is enabled.
FALSE: the circuitry that applies full operating voltage to the PI is disabled.

pi_prebiased
TRUE: the circuitry that applies V_{Sleep} at the PI during the RESTART, RESTART_DELAY, and IDLE states is enabled (see 104.4.6.1).
FALSE: the circuitry that applies V_{Sleep} at the PI is disabled.

pi_sleeping
TRUE: the circuitry that applies V_{Sleep} at the PI during the SETTLE_SLEEP and SLEEP states is enabled (see 104.4.6.1).
FALSE: the circuitry that applies V_{Sleep} at the PI is disabled.

power_stable
TRUE: following inrush, the PSE has begun steady-state operation.
FALSE: the PSE is either not applying full operating voltage or has begun applying full operating voltage but is still in the POWER_UP state.

power_available
TRUE: a compatible PSE class to PD class pairing exists as defined in Table 104–2 and the PSE is able to source the required voltage and power.
FALSE: a valid PSE class to PD class pairing does not exist as defined in Table 104–2 or the PSE is not able to source the required voltage and power.

pse_ready
TRUE: the PSE is ready to probe the link segment.
FALSE: the PSE is not ready to probe the link segment.

pse_reset
Controls the resetting of the PSE state diagram. Condition that is TRUE until such time as the power supply for the device that implements the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE functionality.

valid_class
TRUE: valid class information was received from the PD during SCCP.
FALSE: valid class information was not received from the PD during SCCP.

vsleep_valid
TRUE: V_{PSE} is in the range of V_{Sleep}.
FALSE: V_{PSE} is outside the range of V_{Sleep}.

vsig_valid
TRUE: a valid PD signature has been detected as defined in 104.4.4.2 and 104.4.4.3.
FALSE: an invalid PD signature has been detected as defined in 104.4.4.2 and 104.4.4.3.

104.4.3.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where “stop x_timer” is asserted.

tclass_timer
A timer used to limit the time allowed for classifying a PD (see T_{Class} in Table 104–4).

tdet_timer
A timer used to limit the time allowed for attempting to detect a PD (see T_{det} in Table 104–3).

Table 104–2—PSE power_available matrix

			PSE Class[a]									
			12V unreg		12V reg		24V unreg		24V reg		48V reg	
			0	1	2	3	4	5	6	7	8	9
PD Class[a]	12V unreg	0	x	x	x	x	—	—	—	—	—	—
		1	—	x	x	x	—	—	—	—	—	—
	12V reg	2	—	—	x	x	—	—	—	—	—	—
		3	—	—	—	x	—	—	—	—	—	—
	24V unreg	4	—	—	—	—	x	x	x	x	—	—
		5	—	—	—	—	—	x	x	x	—	—
	24V reg	6	—	—	—	—	—	—	x	x	—	—
		7	—	—	—	—	—	—	—	x	—	—
	48V reg	8	—	—	—	—	—	—	—	—	x	x
		9	—	—	—	—	—	—	—	—	—	x

[a]An ‘x’ denotes a valid PSE to PD Class pairing.

tod_timer
: A timer used to regulate a subsequent attempt to power a PD after an overload condition that causes a fault (see T_{od} in Table 104–4).

tinrush_timer
: A timer used to limit the duration of the inrush event (see T_{Inrush} in Table 104–4).

tmfvdo_timer
: A timer used to monitor the dropout of MFVS (see T_{MFVDO} in Table 104–4).

toff_timer
: A timer used to limit the time the PSE attempts to discharge the PI to the range of V_{Sleep} (see T_{OFF} in Table 104–4). If toff_timer expires during the SETTLE_SLEEP state, an overload condition exists, and the port state diagram enters the OVERLOAD state.

trestart_timer
: A timer used to regulate a subsequent attempt to power a PD after an error condition that does not result in a fault (see $T_{Restart}$ in Table 104–4).

vsig_hold_timer
: A timer used to de-glitch the PD signature voltage valid output in the detection state diagram (see T_{sig_hold} in Table 104–3).

104.4.3.5 Functions

do_classification

This function returns the following variables:

CLASS_TYPE_INFO register:
: The register contains 16 bits of information regarding the type and class of the PD. Refer to Table 104–9 for a description of the contents.

104.4.3.6 State diagram

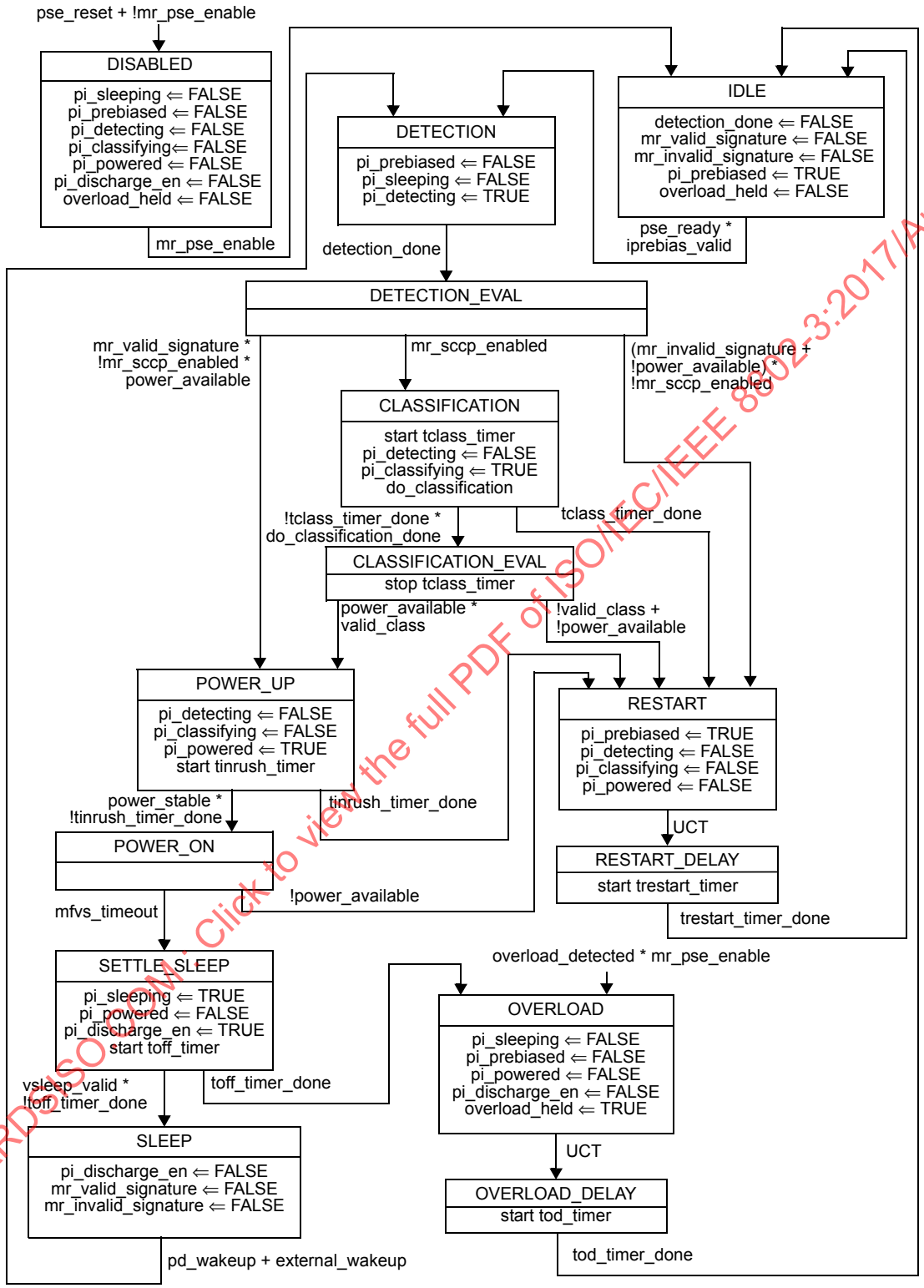


Figure 104–4—PSE state diagram

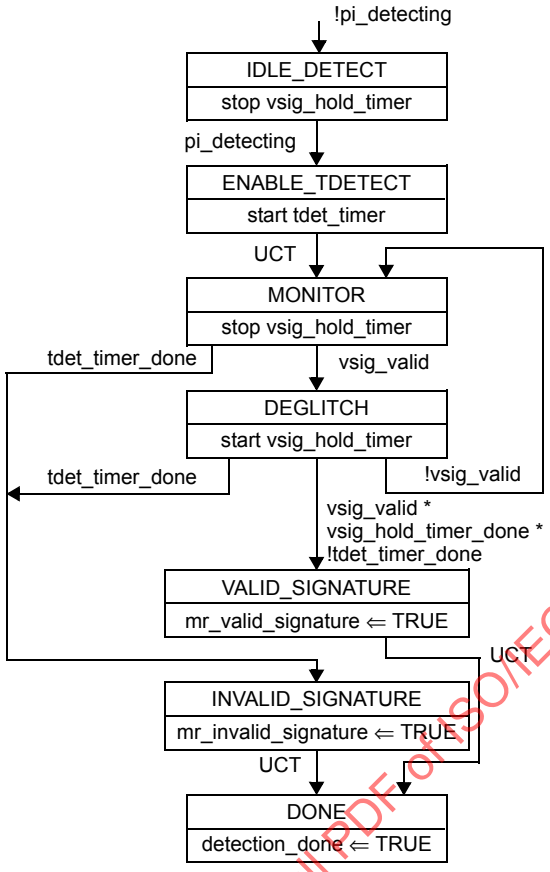


Figure 104–5—Detection state diagram

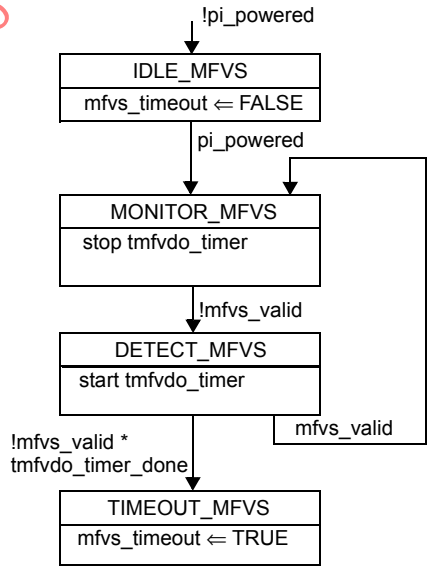


Figure 104–6—MFVS state diagram

104.4.4 PSE detection of a PD

When in the DETECTION state, the PSE shall complete detection of a valid PD signature within T_{det} as specified in Table 104–3. If a valid signature is not detected and classification is not performed, the PSE shall wait at least $T_{Restart}$ before reattempting detection. If a valid signature is detected and classification is not performed, the PSE may proceed to the POWER_UP state. A PSE may successfully detect a PD but then opt not to power the detected PD.

104.4.4.1 Detection probe requirements

All detection currents at the PI shall be within the I_{valid} current range, as specified in Table 104–3, when connected to a valid PD detection signature as specified in Table 104–5. The detection probe shall conform to V_{OC}, I_{SC}, I_{slew}, and C_{out} as specified in Table 104–3.

Table 104–3—PSE PI detection state electrical output requirements

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Open circuit voltage	V_{OC}	V	4.75	5.5	
2	Short-circuit current	I_{SC}	mA	—	24	
3	Valid test probe current	I_{valid}	mA	9	16	
4	Slew rate	I_{slew}	A/ms	—	1	
5	Output capacitance during detection	C_{out}	nF	—	200	
6	Maximum detection time	T_{det}	ms	—	3.11	See 104.4.4
7	Valid PD detection signature range measured at PSE PI	V_{good_PSE}	V	4.05	4.7	See 104.4.4.2
8	Invalid PD detection signature high range measured at PSE PI	$V_{bad\_hi\_PSE}$	V	V_{oc}–0.05	—	See 104.4.4.3
9	Invalid PD detection signature low range measured at PSE PI	$V_{bad\_lo\_PSE}$	V	—	3.7	
10	Signature hold timer for validity	T_{sig_hold}	ms	1	—	See 104.4.4.2

104.4.4.2 Detection criteria

A PSE shall accept as a valid PD signature a link segment with a voltage in the range of V_{good_PSE} for at least T_{sig_hold} in response to a probing current in the range I_{valid} as specified in Table 104–3.

104.4.4.3 Rejection criteria

The PSE shall reject link segments as having an invalid PD signature when those link segments exhibit any of the following characteristics with a probe current, as specified in Table 104–3:

a) Voltage less than or equal to $V_{bad\_lo\_PSE}$ max
b) Voltage greater than or equal to $V_{bad\_hi\_PSE}$ min

A PSE may accept or reject a voltage in the band between $V_{bad\_lo\_PSE}$ max and V_{good_PSE} min and in the band between V_{good_PSE} max and $V_{bad\_hi\_PSE}$ min. The values of these voltages are specified in Table 104–3.

104.4.5 PSE classification of a PD

The ability for the PSE to query the PD in order to determine the PD type and power class requirements of that PD is called classification.

Classification is optional, and is performed using SCCP. See 104.7.

A PSE with SCCP enabled shall complete classification after detection and prior to application of full operating voltage at the PI in a time less than T_{Class} as specified in Table 104–4. If classification is not completed before the T_{Class} timer expires, a new detection cycle shall be completed before any subsequent application of full operating voltage, the PSE shall transition to the RESTART state.

Valid class information is one that returns one of the defined bit patterns in Table 104–9 with a valid CRC8 result.

104.4.6 PSE output requirements

When the PSE provides power to the PSE PI, it shall conform to the electrical limits in Table 104–4.

Under all conditions, a PSE shall present an invalid PD signature with one of the attributes as specified in Table 104–6.

Table 104–4—PSE output requirements

Item	Parameter	Symbol	Unit	Min	Max	Class	Type	Additional information
1	DC output voltage during POWER_ON state	$V_{PSE(PON)}$	V	Class $V_{PSE(min)}$	Class $V_{PSE(max)}$	All	All	See 104.4.6.1 and Table 104–1
2	Continuous output current capability in POWER_ON state		mA	P_{Class}/ V_{PSE}	—	All	All	See Table 104–1
3	Output slew rate dV/dt		V/ms	—	22	All	A, C	See 104.4.6.3
				—	40	All	A, C	During in-rush only
				—	200	All	B	See 104.4.6.3
4	Power feeding ripple and noise:							
4a	1 kHz<*f*<10 MHz		V_{p-p}	—	0.1	All	All	See 104.4.6.3
4b	1 kHz<*f*<10 MHz			—	0.01	All	All	

Table 104–4—PSE output requirements *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Class	Type	Additional information
5	Output current — at short-circuit condition	I_{LIM}	mA	$I_{PI(max)}$	1.41 × $I_{PI(max)}$	All	All	See 104.4.6.2.1
6	Short-circuit time limit	T_{LIM}	ms	10	75	All	All	
7	Inrush time	T_{Inrush}	ms	3.17	3.87	All	All	See 104.4.6.4
8	Classification time	T_{Class}	ms	—	366	All	All	See 104.4.5
9	Turn off time	T_{OFF}	ms	—	500	All	All	See 104.4.6.5
10	DC output voltage during SLEEP state	V_{Sleep}	V	3.15	3.575	All	All	See 104.4.6.1 and 104.4.6.5
11	Overload delay timing	T_{od}	ms	750	—	All	All	
12	Restart timer delay	$T_{Restart}$	ms	500	—			
13	PD MFVS dropout time limit	T_{MFVDO}	ms	300	400			See 104.4.7.1
14	MFVS window time limit	T_{MFVS}	ms	6	—			
15	MFVS current threshold	I_{Hold}	mA	2.5	10			
16	Valid wakeup current signature range	I_{Wakeup}	mA	1.25	1.85			See 104.4.6.2.2
17	Wakeup current hold time required for validity	T_{Wakeup}	ms	0.1	—			
18	Invalid wakeup current signature high range	$I_{Wake-up\_bad\_hi}$	mA	2.5	—			
19	Invalid wakeup current signature low range	$I_{Wake-up\_bad\_lo}$	mA	—	0.5			
20	Output discharge current during SETTLE_SLEEP state	$I_{discharge}$	mA	1.2	24			See 104.4.6.2

Table 104–4—PSE output requirements *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Class	Type	Additional information
21	DC output voltage during the DISABLED, OVERLOAD, and OVERLOAD_DELAY states	$V_{Disable}$	V	—	1	All	All	See 104.4.6.1
22	Disable time	$T_{Disable}$	ms	—	500	All	All	See 104.4.6.6

104.4.6.1 Output voltage

A PSE operating in the POWER_ON state shall apply a voltage in the range of $V_{PSE(PON)}$ at the PI. A PSE shall apply a voltage at the PI in the range of $V_{Disable}$ when in the OVERLOAD, OVERLOAD_DELAY, and DISABLED states (see 104.4.6.5).

The PSE shall apply a voltage at the PI in the range of V_{Sleep} while operating in the SLEEP, RESTART, RESTART_DELAY, and IDLE states (see Table 104–4).

A PSE operating in the SETTLE_SLEEP state shall discharge the PSE PI to the range of V_{Sleep} within a time less than T_{OFF} max.

104.4.6.2 Output current

A PSE operating in the POWER_ON state shall enter the SETTLE_SLEEP state if a valid MFVS is not present at the PI.

A PSE operating in the SETTLE_SLEEP state shall discharge the PI to the range of V_{Sleep} with a current in the range of $I_{discharge}$.

During the POWER_UP state, PSE output shall not exceed I_{LIM} max.

104.4.6.2.1 Output current—at overload condition

During operation in the POWER_UP and POWER_ON states, the PSE shall limit the current to I_{LIM} for a duration of up to T_{LIM} in order to account for PSE dV/dt transients at the PI as specified in Table 104–4.

If I_{PSE} exceeds I_{LIM} min during the POWER_ON state, the PSE output voltage may drop below $V_{PSE(PON)}$ min.

During operation in any state other than POWER_UP or POWER_ON when the PSE is enabled, the PSE shall limit I_{PSE} to less than I_{SC} as specified in Table 104–3 for a duration of up to T_{LIM}.

If the PSE is limiting current in any state when pi_powered, pi_sleeping or pi_prebias are true, within T_{LIM} of the initiation of current limiting, overload_detected is set TRUE and power removal from the PI shall begin.

Measurements of I_{PSE} during a short-circuit condition shall be made 1 ms after the initial transient to allow for settling.

104.4.6.2.2 Wakeup current signature detection

A PSE shall transition from the SLEEP state to the DETECTION state when I_{PSE} is in the valid range of I_{Wakeup} for a minimum of T_{Wakeup} (see Table 104–4).

A PSE operating in the SLEEP state shall remain in the SLEEP state if I_{PSE} is greater than $I_{Wakeup\_bad\_hi}$ or less than $I_{Wakeup\_bad\_lo}$. A PSE may consider a PD wakeup request valid or invalid if I_{PSE} is in the band between $I_{Wakeup\_bad\_hi}$ and I_{Wakeup} max or the band between I_{Wakeup} min and $I_{Wakeup\_bad\_lo}$.

104.4.6.2.3 Output current requirement during idle

The PSE output current during the IDLE state shall be defined as valid if it less than I_{Wakeup} max for at least T_{Wakeup} min (see Table 104–4). A PSE may define its output current during the IDLE state as valid if the current is in the range between I_{Wakeup} max and $I_{Wakeup\_bad\_hi}$ for at least T_{Wakeup} min.

A PSE may define its output current during the IDLE state as invalid if the current is in the range between I_{Wakeup} max and $I_{Wakeup\_bad\_hi}$. A PSE shall consider its output current during the IDLE state to be invalid if the current is greater than $I_{Wakeup\_bad\_hi}$.

104.4.6.3 Power feeding ripple and transients

The ripple and transient limits specified in Table 104–4, items (4) and (3) respectively, are meant to preserve data integrity.

A digital oscilloscope or data acquisition module with a differential probe is used to observe the voltage at the MDI/PI of the PSE device under test (DUT) as shown in Figure 104–7. The input impedance, $Z_{in}(f)$, and transfer function, $H_1(f)$, of the differential probe are specified by Equation (104–1) and Equation (104–2), respectively. When measuring the ripple voltage for a Type A or Type C PSE as specified by Table 104–4 item (4a), f_1 = 31.8 kHz ± 1%. When measuring the ripple voltage for a Type B PSE as specified in Table 104–4 item (4a), f_1 = 318 kHz ± 1%.

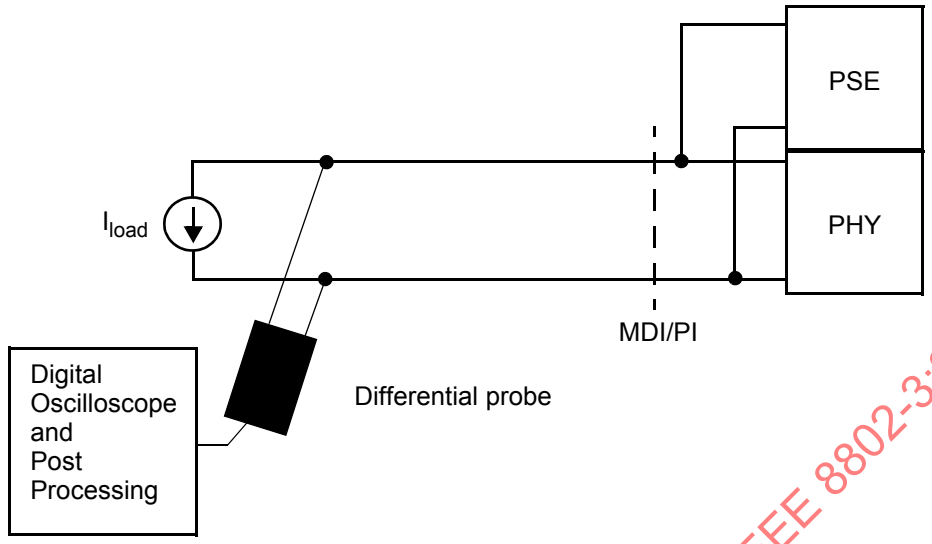


Figure 104–7—PSE ripple voltage test fixture

$$Z_{in}(f) = 100\Omega \pm 0.1\% \times \frac{\sqrt{f^2 + f_1^2}}{f} \quad (104\text{–}1)$$

$$H_1(f) = \frac{f}{\sqrt{f^2 + f_1^2}} \quad (104\text{–}2)$$

When measuring the ripple voltages for a Type A or Type C PSE as specified by Table 104–4 item (4b), the voltage observed at the MDI/PI with the differential probe where f_1 = 31.8 kHz ± 1% is post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 1 MHz ± 1%.

When measuring the ripple voltages for a Type B PSE as specified by Table 104–4 item (4b), the voltage observed at the MDI/PI with the differential probe where f_1 = 318 kHz ± 1% is post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 10 MHz ± 1%.

$$H_2(f) = \frac{f}{\sqrt{f^2 + f_2^2}} \quad (104\text{–}3)$$

104.4.6.4 Inrush time

The specification for T_{Inrush} in Table 104–4 applies to the PSE power-up time allowed for a PD after completion of detection and optional classification. If full operating voltage is applied within T_{Inrush} min, the PSE shall enter the POWER_ON state. If full operating voltage is not applied within T_{Inrush} max, a new detection cycle shall be initiated after a delay of $T_{Restart}$ before any subsequent application of full operating voltage. If full operating voltage is applied within the range of T_{Inrush}, the PSE may enter the POWER_ON state or begin a new detection cycle after a delay of $T_{Restart}$.

104.4.6.5 Turn off time

The specification for T_{OFF} in Table 104–4 applies to the discharge time from V_{PSE} in the POWER_ON state to V_{Sleep}. In addition, it is recommended that the PI be discharged when the PSE is not enabled. T_{OFF} starts

when V_{PSE} drops 1 V below the steady-state full operating voltage value after the pi_powered variable is set to FALSE. T_{OFF} ends when $V_{PSE} < V_{Sleep}$ max.

104.4.6.6 Disable time

The specification for $T_{Disable}$ in Table 104–4 shall apply to the discharge time from V_{PSE} to $V_{Disable}$ with a test resistor of 320 kΩ attached to the PI. $T_{Disable}$ starts when V_{PSE} drops 1 V below the steady-state value after the pi_powered, pi_classifying, pi_detecting, pi_prebiased, and pi_sleeping variables are set to FALSE (see Figure 104–4). $T_{Disable}$ ends when V_{PSE} is less than or equal to $V_{Disable}$ max.

104.4.6.7 Continuous output power in POWER_ON state

P_{Class} is the minimum continuous class power that the PSE shall be capable of supplying, as defined in Table 104–1.

Measurement of P_{Class} shall be averaged using a uniform sliding window with a width of 1 s.

A PSE may remove power from the PI when more than P_{Class} is sourced.

104.4.7 PSE power removal

While the PSE is operating in the POWER_ON state, full operating voltage shall be removed from the PSE PI in the absence of the PD MFVS or if overload_detected is TRUE.

104.4.7.1 PSE MFVS requirements

MFVS shall be defined as being present in the POWER_ON state when I_{PSE} is greater than or equal to I_{Hold} max for a minimum of T_{MFVS}.

MFVS may be defined as present or absent in the POWER_ON state if I_{PSE} is in the range of I_{Hold}.

MFVS shall be defined as absent in the POWER_ON state if I_{PSE} is less than or equal to I_{Hold} min. The PSE-PI Voltage shall be reduced to the range of V_{Sleep} when MFVS has been absent for a duration greater than T_{MFVDO}.

104.5 Powered Device (PD)

A PD is the portion of a device that is either drawing power or requesting power by participating in the PD detection or classification algorithms. A device that is capable of becoming a PD may have the ability to draw power from an alternate power source. A PD requiring power from the PI may simultaneously draw power from an alternate power source.

A PD is specified at the point of the physical connection to the PI. Limits defined for a PD are specified at the PI, not at any point internal to the PD, unless specifically stated.

104.5.1 PD types

For PoDL systems there are four types of PDs—Type A, Type B, Type C, and Type D consistent with 104.1.3.

104.5.2 PD classes

A PD shall comply with the voltage and power requirements listed in Table 104–1 for the relevant class.

104.5.3 PD state diagram

The PD state diagram specifies the externally observable behavior of a PD. The PD shall provide the behavior of the state diagram shown in Figure 104–8.

104.5.3.1 Overview

A falling edge of the PD input voltage through V_{sig_enable} enables a voltage signature, as defined in 104.5.4. When the input voltage rises through the $V_{sig\_disable}$ the PD disables its voltage signature.

A PD requests detection and wakeup while the voltage signature is enabled by presenting a valid wakeup current signature. SCCP may also be used for communication with the PD by the PSE when the voltage signature is enabled.

A rising edge through the V_{On} threshold causes the PD to enable MDI power to the load after a delay of T_{power_dly}. A falling edge through the V_{Off} threshold causes the PD to disable MDI power.

104.5.3.2 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in 21.5.

104.5.3.3 Variables

The PD state diagram uses the following variables:

disconnect_pd
: TRUE: the PD no longer requires full operating voltage from the PI and has reduced its port current below the MFVS threshold current.
FALSE: the PD still requires full operating voltage from the PI.

enable_mdi_pwr
: TRUE: the PD is enabled and ready to consume full power from the PI.
FALSE: the PD is disabled or not ready to consume full power from the PI.

fault_detected
: TRUE: the PD no longer requires power as the result of an implementation-specific error condition.
FALSE: no fault has been detected.

pd_fault
: TRUE: following the application of full operating voltage at the PI, the PD has gone offline as the result of an error condition.
FALSE: following the application of full operating voltage at the PI, no fault has been detected.

pd_sccp_enabled
: TRUE: during detection, a PSE reset pulse has been detected by the PD and a SCCP serial transaction is pending.
FALSE: during detection, no PSE reset pulse has been detected by the PD.

pd_reset
: An implementation-specific control variable that unconditionally resets the PD state diagram to the RESET state.
TRUE: the device is in reset.
FALSE: the device is not in reset (default).

present_det_sig
A variable that controls the PD detection signature as specified in 104.5.4.
TRUE: the detection signature is to be applied to the PD PI.
FALSE: the detection signature is not to be applied to the PD PI.

present_iwakeup
TRUE: the wakeup signature (I_{Wakeup_PD}) is to be applied to the PD PI.
FALSE: the wakeup signature (I_{Wakeup_PD}) is not to be applied to the PD PI.

present_mfvs
TRUE: the MFVS is to be applied to the PD PI.
FALSE: the MFVS is not to be applied to the PD PI.

sccp_reset_pulse
TRUE: during detection, a SCCP reset pulse per Figure 104–10 as described in 104.7.1.1 has been received by the PD.
FALSE: during detection, a SCCP reset pulse has not been received by the PD.

V_{Off}
PD turn off threshold voltage (see Table 104–7).

V_{On}
PD turn on threshold voltage (see Table 104–7).

V_{PD}
The voltage measured at the PI of the PD.

$V_{sig\_disable}$
PD signature disable threshold voltage (see Table 104–5).

V_{sig_enable}
PD signature enable threshold voltage (see Table 104–5).

wakeup
TRUE: the PD requires the full operating voltage at the PI.
FALSE: the PD is ready to go to sleep.

104.5.3.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop x_timer” is asserted.

tpower_dly_timer
A timer used to prevent a PD from drawing more than inrush current during the PSE’s POWER_UP state (see T_{power_dly} in Table 104–7).
sccp_watchdog_timer
A timer used to limit the time in the DO_CLASSIFICATION state in the event serial communication between the PSE and PD is idle or stalled (see $T_{SCCP\_watchdog}$ in Table 104–7).

104.5.3.5 Functions

do_sccp
This function returns the following variable to the PSE:

CLASS_TYPE_INFO register: refer to Table 104–9 for a description of the contents.

104.5.3.6 State diagram

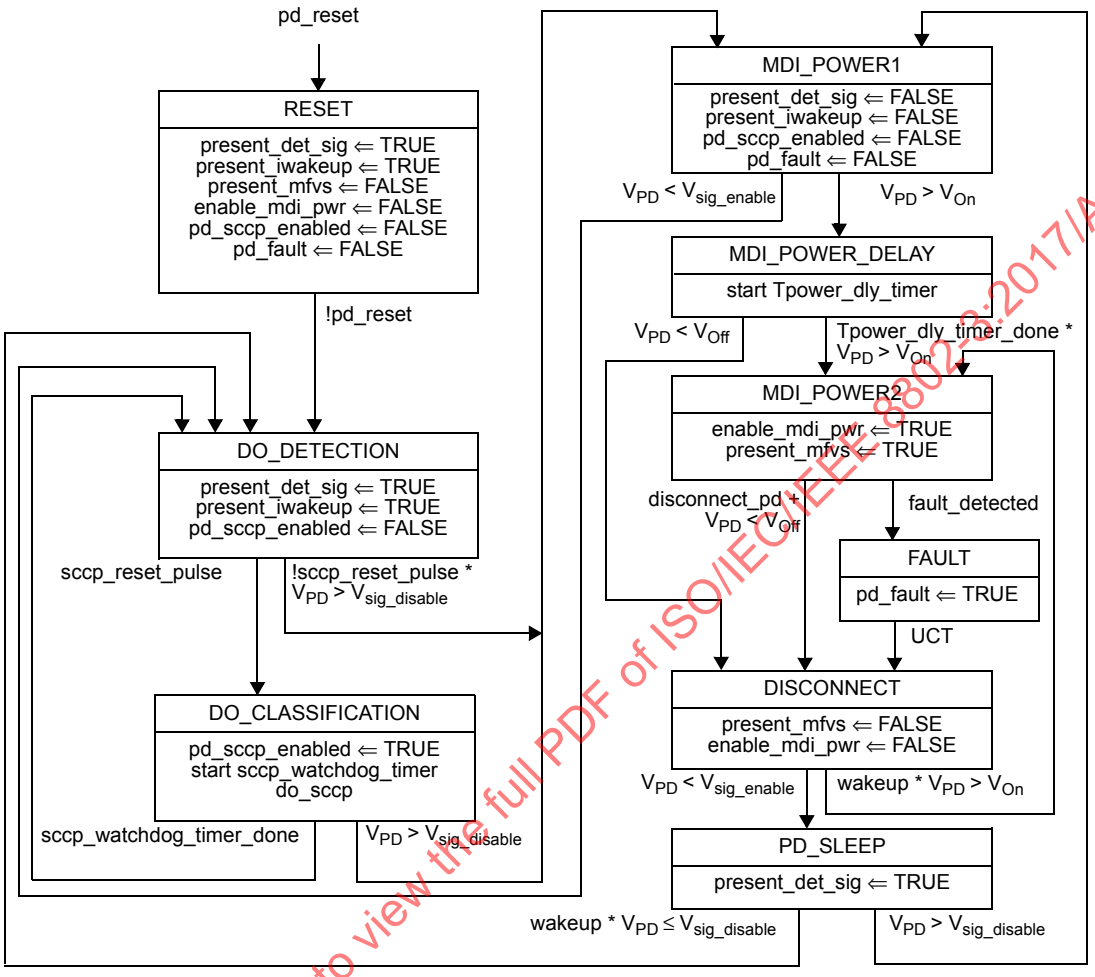


Figure 104–8—PD state diagram

104.5.4 PD signature

Class 0 and Class 1 PDs, or PDs that do not implement classification shall enable a valid detection signature when V_{PD} is less than V_{sig_enable} min and may enable a valid detection signature when V_{PD} is less than V_{sig_enable} max. A PD that presents an invalid detection signature greater than V_{bad_hi} max as specified in Table 104–6 shall implement classification as specified in 104.7.

When V_{PD} is greater than $V_{sig\_disable}$ a PD shall remove the current draw of the detection signature.

The detection signature shall consist of a current limited voltage V_{good} per Table 104–5 when measured by the PSE.

A valid PD detection signature shall have all of the characteristics of Table 104–5.

A non-valid PD detection signature shall have one of the characteristics in Table 104–6.

A PD that presents a signature within the limits set out in Table 104–5 is assured to pass detection, while a PD that presents one of the signature characteristics of Table 104–6 is assured to fail detection.

Table 104–5—Valid PD detection signature characteristics, measured at PD PI

Parameter	Conditions	Min	Max	Unit
V_{good}	7 mA < I_{PD} < 17 mA, PD exiting RESET state	4.05	4.55	V
$I_{signature\_limit}$	V_{PD} < $V_{sig\_disable}$ max	—	24	mA
$V_{sig\_disable}$	V_{PD} rising	4.6	5.75	V
V_{sig_enable}	V_{PD} falling	3.6	4.3	V

Table 104–6—Non-valid PD detection signature characteristics, measured at PD PI

Parameter	Conditions	Min	Max	Unit
V_{bad_hi}	7 mA < I_{PD} < 17 mA, PD exiting RESET state	5.15	—	V
V_{bad_lo}	7 mA < I_{PD} < 17 mA, PD exiting RESET state	—	3.7	V

104.5.5 PD classification and mutual identification between the PSE and PD

A PD may be classified by the PSE based on SCCP information provided by the PD. The intent of PD classification is to provide information about the voltage and power required by the PD during operation. SCCP classification may also be used to establish mutual identification between a PSE and a PD. See 104.7 for more information about SCCP.

104.5.6 PD power

The PD shall operate within the characteristics in Table 104–7.

Table 104–7—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD type	Additional information
1	Input current dI/dt		A/ms	—	1	A, C	See 104.5.6.4
				—	10	B	
2	Input voltage dV/dt		V/ms	—	20	A, C	
				—	200	B	
3	Ripple voltage						
3a	1 kHz < f < 10 MHz		V_{p-p}	—	0.1	All	See 104.5.6.4
3b	1 kHz < f < 10 MHz			—	0.01	All	

Table 104–7—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD type	Additional information
4a	Power supply turn on voltage (unregulated 12 V classes)	V_{On}	V	—	5.75	All	See 104.5.6.2
4b	Power supply turn on voltage (regulated 12 V classes)			—	13.6		
4c	Power supply turn on voltage (unregulated 24 V classes)			—	11.4		
4d	Power supply turn on voltage (regulated 24 V classes)			—	24.7		
4e	Power supply turn on voltage (regulated 48 V classes)			—	45.6		
5a	Power supply turn off voltage (unregulated 12 V classes)	V_{Off}	V	3.6	—		
5b	Power supply turn off voltage (regulated 12 V classes)			9.56	—		
5c	Power supply turn off voltage (unregulated 24 V classes)			7.97	—		
5d	Power supply turn off voltage (regulated 24 V classes)			19.5	—		
5e	Power supply turn off voltage (regulated 48 V classes)			33	—		
6a	Input Capacitance during DO_DETECTION, MDI_POWER1, and MDI_POWER_DELAY states	C_{IN}	µF	—	10		Classes 1 to 3 and 5 to 9
				—	5		Class 4
6b	Input capacitance during DO_CLASSIFICATION state	C_{IN_Class}		—	0.2		All classes
7	Inrush enable delay time	T_{power_dly}	ms	1.46	—		See 104.5.6.2
8	PD MFVS duration	T_{MFVS_PD}	ms	10	—		See 104.5.7
9	MFVS current threshold limit	I_{hold_PD}	mA	11	—		
10	Power supply voltage during PD_SLEEP state	V_{Sleep_PD}	V	3.1	3.575		See 104.5.6.2

Table 104–7—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD type	Additional information
11	Sleep current	I_{Sleep_PD}	mA	—	0.1		See 104.5.6.3
12	Wakeup current	I_{Wakeup_PD}	mA	1.3	1.8		See 104.5.6.3
13	Input current not related to inrush	I_{PD_pwr1}	mA	—	5		See 104.5.6.3
14	Wakeup current hold time required for validity	T_{Wakeup_PD}	ms	0.2	—		See 104.5.6.3
15	SCCP watchdog timeout	$T_{SCCP\_watch-dog}$	ms	150	200		See 104.5.5

104.5.6.1 PD discharge

At a delay of T_{OFF} max (see Table 104–4) after disconnection from the PSE, a PD shall not source greater than 410 µJ out of its PI until V_{PD} drops below V_{Sleep_PD} max.

104.5.6.2 PD input voltage

The PD shall turn on at a voltage less than or equal to V_{On} max and with a delay greater than T_{power_dly} min. After the PD turns on, the PD shall stay on over the range from V_{PD} min to V_{PSE} max. The PD shall turn off at a voltage in the range of V_{PD} min to V_{Off} min. Table 104–1 defines the values for V_{PD} min and V_{PSE} max. Table 104–7 defines the values for V_{On}, T_{power_dly}, and V_{Off}.

The PD shall turn on or off without startup oscillation and within the first trial when a voltage in the range of V_{PSE} (as defined in Table 104–1) is applied with a series resistance within the range of valid dc loop resistance (see 104.2).

The PD shall operate in the PD_SLEEP state with an input voltage greater than V_{Sleep_PD} min as specified in Table 104–7.

When the input voltage is greater than $V_{sig\_disable}$, then the signature is disabled.

104.5.6.3 Input current

During operation in the DISCONNECT and PD_SLEEP states, the PD shall not draw current in excess of I_{Sleep_PD} as specified in Table 104–7.

A PD that requires detection and application of power shall draw current in the range of I_{Wakeup_PD} for at least T_{Wakeup_PD} when V_{PD} is within the range of V_{Sleep_PD} as specified in Table 104–7.

A PD shall draw less than I_{PD_pwr1} max of current for a constant PD input voltage between $V_{sig\_disable}$ max and V_{On} min.

104.5.6.4 PD ripple and transients

The specifications for ripple and transients in Table 104–7 apply to the voltage or current at the PD PI generated by the PD circuitry. Ripple and transient limits are provided to preserve data integrity.

The PD DUT is connected to a power supply through a dc bias coupling network as shown in Figure 104–9. The ripple and transient specifications for a Type A or Type C PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Equation (96–11a), and over the range of P_{PD}. The ripple and transient specifications for a Type B PD shall be met for all operating voltages in the range of V_{PD} sourced through a dc bias coupling network with MDI return loss as specified by Clause 97, and over the range of P_{PD}.

A digital oscilloscope or data acquisition module with a differential probe is used to observe the voltage at the MDI/PI. The input impedance, $Z_{in}(f)$, and transfer function, $H_1(f)$, of the differential probe are specified by Equation (104–1) and Equation (104–2), respectively. When measuring the ripple voltage for a Type A or Type C PD as specified by Table 104–7 item (3a), f_1 = 31.8 kHz ± 1%. When measuring the ripple voltage for a Type B PD as specified by Table 104–7 item (3a), f_1 = 318 kHz ± 1%.

When measuring the ripple voltages for a Type A or Type C PD as specified by Table 104–7 item (3b), the voltage observed at the MDI/PI with the differential probe where f_1 = 31.8 kHz ± 1% shall be post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 1 MHz ± 1%. When measuring the ripple voltages for a Type B PD as specified by Table 104–7 item (3b), the voltage observed at the MDI/PI with the differential probe where f_1 = 318 kHz ± 1% shall be post-processed with transfer function $H_2(f)$ specified in Equation (104–3) where f_2 = 10 MHz ± 1%.

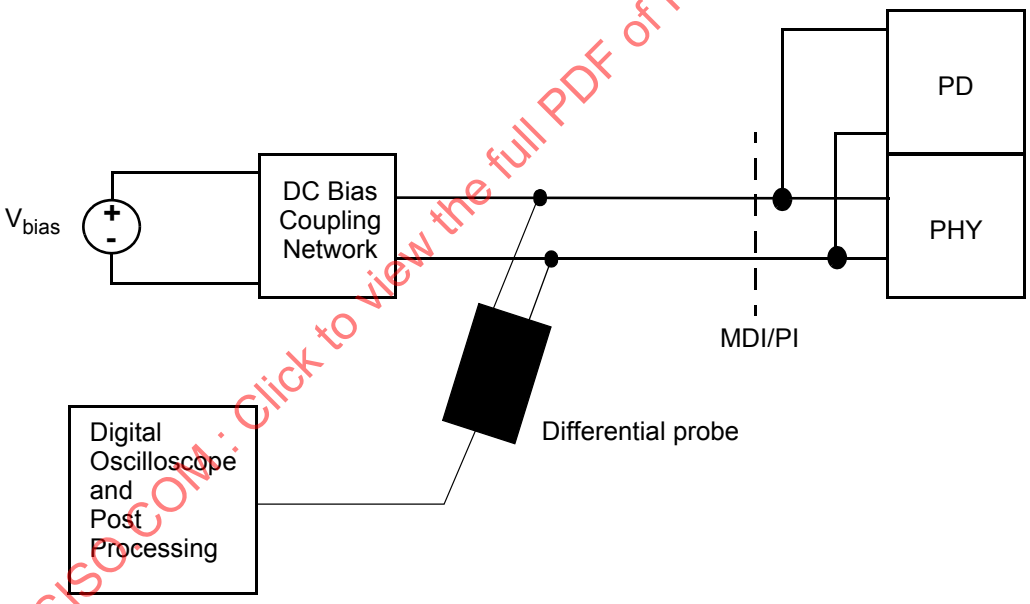


Figure 104–9—PD ripple voltage test fixture

104.5.6.5 Input average power

The maximum average power, $P_{PD(max)}$ in Table 104–1, shall be calculated using a uniform sliding window with a width of 1 s.

104.5.6.6 PD stability

When any voltage between V_{PSE} min and V_{PSE} max (with R_{Loop_max} in series) is applied to the PI of the PD, P_{PD} is defined as shown in Equation (104–4).

$$P_{PD} = (V_{PD} \times I_{PD}) \text{ (Watts)} \quad (104–4)$$

where

P_{PD} is the input power at the PD PI
V_{PD} is the input voltage at the PD PI
I_{PD} is the input current to the PD

NOTE—When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input.

104.5.7 PD Maintain full voltage

In order to signal the PSE to maintain full operating voltage, the PD shall provide a valid MFVS at the PI. The MFVS shall consist of current draw equal to or greater than I_{hold_PD} for a minimum duration of T_{MFVS_PD} measured at the PD PI followed by an allowed MFVS dropout for no longer than T_{MFVDO} min. PDs that do not require full operating voltage at the PI shall remove the current draw of the MFVS from the PI.

104.6 Additional electrical specifications

104.6.1 Isolation

In order to prevent the formation of a ground loop, a PD shall provide at least 1 MΩ dc isolation between all accessible external conductors, including frame ground (if any), and all MDI leads, when measured using a 5 V ± 20% source voltage. Any equipment that can be connected to a PD through a non-MDI connector that is not isolated from the MDI leads must provide isolation between all accessible external conductors, including frame ground (if any), and the non-MDI connector, so as not to negate the dc isolation provided by the PD.

104.6.2 Fault tolerance

The PI for Type A, Type B, and Type C PSEs and PDs shall meet the fault tolerance requirements as specified in 96.8.3.

A PD shall not be damaged when connected to any PSE as defined in 104.4.

The PSE PI shall withstand without damage the application of short circuits between the wires within the cable for an indefinite period of time.

104.7 Serial communication classification protocol (SCCP)

Implementation of SCCP by PSEs and PDs that present a valid detection signature is optional. PDs that present an invalid detection signature as specified in Table 104–6 shall implement SCCP. The PSE acts as a master during the SCCP exchange, controlling the PD that acts as the slave device. SCCP is a current-sinking, wired-OR (e.g., open-drain or open-collector), half-duplex bidirectional serial data bus. The PSE sources the required pull-up current. The logic high voltage is limited by the voltage signature device at the PD. PDs can derive power from the PSE's pull-up current during classification via the PD PI.

104.7.1 SCCP signaling

SCCP uses the following signal types in order to ensure data integrity: reset pulse, presence pulse, Write 0, Write 1, Read 0, and Read 1. The PSE initiates all of these signals.

104.7.1.1 Initialization procedure—reset and presence pulses

All SCCP communication with a PD shall begin with an initialization sequence that consists of a reset pulse from the PSE followed by a presence pulse from the PD. This is illustrated in Figure 104–10. See Table 104–8 for requirements on the timing relationships.

During the initialization sequence the PSE shall transmit the reset pulse by first driving V_{PSE} low and then releasing to the pull up at t_{RSTL}. The PSE shall then go into receive mode (RX). When the PD detects the rising edge at the PD PI, it shall wait t_{PDH} and then transmit a presence pulse by pulling V_{PD} low for t_{PDL}. Presence data from the PD shall be valid for the entire time window defined by t_{MSP} following the rising edge that terminated the reset pulse. Therefore, the PSE should sample the subsequent voltage within t_{MSP} from the completion of the preceding rising edge at its PI.

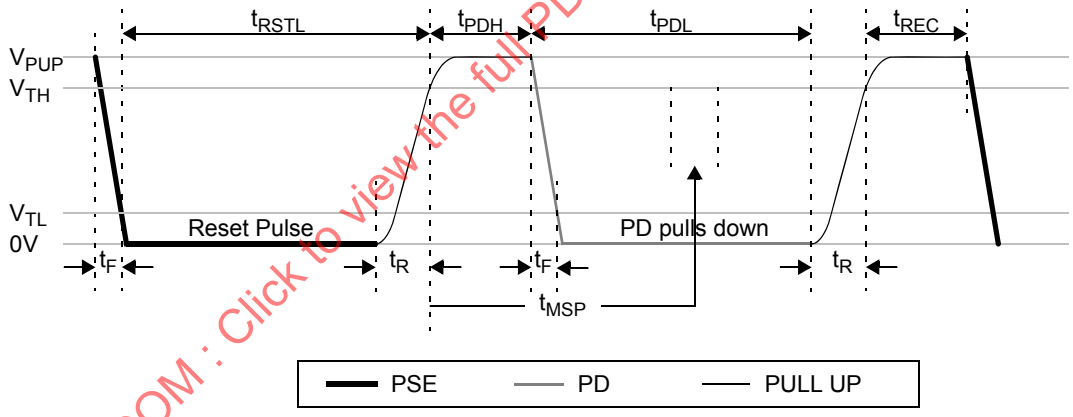


Figure 104–10—Reset command timing diagram

104.7.1.2 Write time slots

There are two types of write time slots: Write 1 and Write 0 time slots. Figure 104–11 illustrates Write 0/1 timing diagrams. The PSE shall use a Write 1 time slot to transmit a logic 1 to the PD and a Write 0 time slot to transmit a logic 0 to the PD. All write time slots shall be t_{SLOT} in duration. The PSE shall initiate both types of write time slots by pulling V_{PSE} low.

To generate a Write 1 time slot, after pulling V_{PSE} low, the PSE shall pull up V_{PSE} within the range of t_{W1L}. To generate a Write 0 time slot, after pulling the V_{PSE} low, the PSE shall pull up V_{PSE} within the range of t_{W0L}. The PD shall sample the V_{PD} within the range of t_{ssw} after the falling edge during a Write 1 or Write 0 operation.

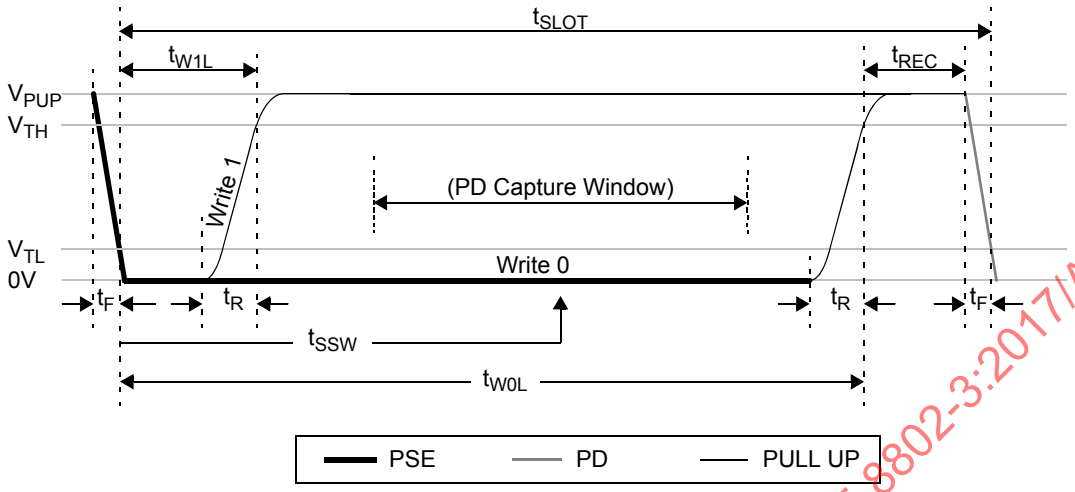


Figure 104–11—Write 0/1 slot timing diagram

104.7.1.3 Read time slots

Figure 104–12 illustrates Read 0/1 timing diagrams. The PD can only transmit data to the PSE when the PSE issues read time slots. Therefore, the PSE shall generate read time slots immediately after issuing a function command, which requires data from the PD so that the PD can provide the requested data. In addition, the PSE can generate read time slots after issuing a manufacturer specific function command in order to determine the status of a commanded operation.

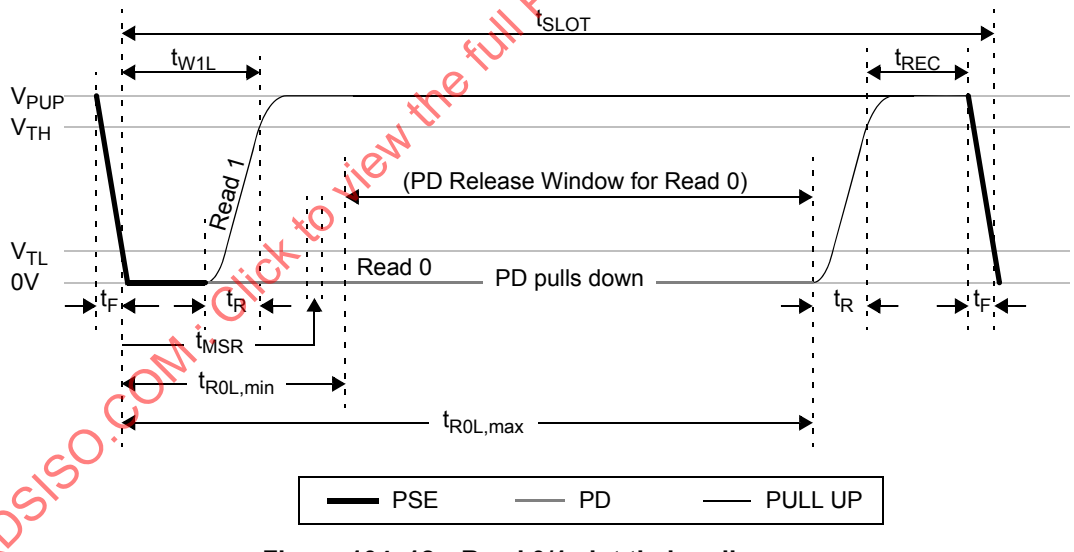


Figure 104–12—Read 0/1 slot timing diagram

All read time slots shall be t_{SLOT} in duration. The PSE shall initiate a read time slot by pulling V_{PSE} low and then pulling-up V_{PSE} within t_{W1L}. After the PSE initiates the read time slot, the PD shall begin transmitting a 1 or 0 at its PI. The PD shall transmit a 1 by leaving V_{PD} high and transmit a 0 by pulling V_{PD} low. When transmitting a 0, the PD shall hold V_{PD} low and then release V_{PD} within t_{R0L}. V_{PSE} and V_{PD} will be pulled back to the high idle state by the PSE's pull-up current. Output data from the PD is valid for t_{MSR} after the falling edge that initiated the read time slot. Therefore, the PSE shall release V_{PSE} and then sample the