

INTERNATIONAL STANDARD

**Qi Specification version 2.0 –
Part 10: MPP System Specification**

IECNORM.COM : Click to view the full PDF of IEC 63563-10:2025



THIS PUBLICATION IS COPYRIGHT PROTECTED

Copyright © 2025 IEC, Geneva, Switzerland

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either IEC or IEC's member National Committee in the country of the requester. If you have any questions about IEC copyright or have an enquiry about obtaining additional rights to this publication, please contact the address below or your local IEC member National Committee for further information.

IEC Secretariat
3, rue de Varembe
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigendum or an amendment might have been published.

IEC publications search - webstore.iec.ch/advsearchform

The advanced search enables to find IEC publications by a variety of criteria (reference number, text, technical committee, ...). It also gives information on projects, replaced and withdrawn publications.

IEC Just Published - webstore.iec.ch/justpublished

Stay up to date on all new IEC publications. Just Published details all new publications released. Available online and once a month by email.

IEC Customer Service Centre - webstore.iec.ch/csc

If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: sales@iec.ch.

IEC Products & Services Portal - products.iec.ch

Discover our powerful search engine and read freely all the publications previews, graphical symbols and the glossary. With a subscription you will always have access to up to date content tailored to your needs.

Electropedia - www.electropedia.org

The world's leading online dictionary on electrotechnology, containing more than 22 500 terminological entries in English and French, with equivalent terms in 25 additional languages. Also known as the International Electrotechnical Vocabulary (IEV) online.

IECNORM.COM : Click to view the full text of IEC 60363-10:2025

INTERNATIONAL STANDARD

**Qi Specification version 2.0 –
Part 10: MPP System Specification**

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 29.240.99; 35.240.99

ISBN 978-2-8327-0183-6

Warning! Make sure that you obtained this publication from an authorized distributor.

INTERNATIONAL ELECTROTECHNICAL COMMISSION

QI SPECIFICATION VERSION 2.0 –
Part 10: MPP System Specification**FOREWORD**

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) IEC draws attention to the possibility that the implementation of this document may involve the use of (a) patent(s). IEC takes no position concerning the evidence, validity or applicability of any claimed patent rights in respect thereof. As of the date of publication of this document, IEC had not received notice of (a) patent(s), which may be required to implement this document. However, implementers are cautioned that this may not represent the latest information, which may be obtained from the patent database available at <https://patents.iec.ch>. IEC shall not be held responsible for identifying any or all such patent rights.

IEC 63563-10 has been prepared by technical area 15: Wireless Power Transfer, of IEC technical committee 100: Audio, video and multimedia systems and equipment. It is an International Standard.

It is based on *Qi Specification version 2.0, MPP System Specification* and was submitted as a Fast-Track document.

The text of this International Standard is based on the following documents:

Draft	Report on voting
100/4254/FDIS	100/4275/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

The structure and editorial rules used in this publication reflect the practice of the organization which submitted it.

This document was developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

IECNORM.COM : Click to view the full PDF of IEC 63563-10:2025



Qi Specification

MPP System Specification

Version 2.0

April 2023

IECNORM.COM : Click to view the full PDF of IEC 63563-10:2025

DISCLAIMER

The information contained herein is believed to be accurate as of the date of publication, but is provided “as is” and may contain errors. The Wireless Power Consortium makes no warranty, express or implied, with respect to this document and its contents, including any warranty of title, ownership, merchantability, or fitness for a particular use or purpose. Neither the Wireless Power Consortium, nor any member of the Wireless Power Consortium will be liable for errors in this document or for any damages, including indirect or consequential, from use of or reliance on the accuracy of this document. For any further explanation of the contents of this document, or in case of any perceived inconsistency or ambiguity of interpretation, contact: info@wirelesspowerconsortium.com.

RELEASE HISTORY

Specification Version	Release Date	Description
2.0	April 2023	First release of this v2.0 specification.

Table of Contents

Table of Contents	2
List of Figures	6
List of Tables	9
1 General Description	10
1.1 Introduction	10
1.1.1 Scope	10
1.1.2 Document organization	10
1.1.3 Design goals	10
1.1.4 BPP and MPP interoperability	12
1.1.5 Related documents	12
1.2 Architectural overview	13
1.2.1 System Description	13
1.2.2 System block diagrams	14
1.3 Glossary	16
1.3.1 Definitions	16
1.3.2 Acronyms	17
1.3.3 Symbols	17
1.4 System Model vs Spec	18
2 Authentication Protocol	19
2.1 Authentication	19
3 Coil Design	20
3.1 Introduction and Background	20
3.2 PTx Coil System Model	20
3.2.1 Mechanical Construction	20
3.2.2 Electrical Properties	31
3.3 PRx Coil System Model	33
3.3.1 Mechanical Construction	33
3.3.2 Electrical Properties	42

3.4	Properties of Mated Coil System Models	43
3.4.1	Electrical measurement under mated conditions	43
3.5	Coil Specifications.....	44
3.5.1	PRx Coil Specifications	44
3.5.2	PTx Coil Specifications.....	50
4	Power Delivery.....	57
4.1	Power Profiles (BPP + MPP)	57
4.1.1	Specifications.....	57
4.1.2	Recommendations.....	57
4.1.3	Specification Notes	57
4.2	Power Receiver Functional Block Diagram	58
4.2.1	System Model	58
4.3	Power Transmitter Functional Block Diagram	65
4.3.1	System Model	65
4.4	Operating Frequency	68
4.4.1	System Model	68
4.4.2	Specifications.....	68
4.5	Object Detection	68
4.5.1	System Model	68
4.5.2	Specifications.....	69
4.6	Digital Pings 128kHz/360kHz	69
4.6.1	Need For Digital Pings 128kHz / 360kHz.....	69
4.6.2	Specifications.....	76
4.7	K Estimation	78
4.7.1	System Model	78
4.7.2	Specifications.....	82
4.8	Output Impedance and Load Transients	83
4.8.1	System Model	83
4.9	Set Pr_max	86
4.9.1	Background.....	86
4.9.2	System Model	86
4.9.3	PTx Specifications	92
4.9.4	PTx Specification Notes.....	92
4.10	Power Transfer Control.....	92
4.10.1	Intro and Background (Informative)	92

4.10.2	System Model	92
4.10.3	End-to-End Control Specifications	98
4.11	Mitigation of Side Effects of Cd at MPP Frequency	101
4.11.1	System Model	101
4.11.2	Specifications.....	104
4.12	Cloak.....	104
4.13	Common-mode Noise	104
5	Communications Physical Layer	105
5.1	Introduction	105
5.2	Frequency Shift Keying (PTx to PRx)	105
5.2.1	System Model	106
5.2.2	Frequency Shift Keying Specifications	108
5.3	Amplitude Shift Keying (PRx to PTx)	109
5.3.1	Modulation Scheme	109
5.3.2	System Model	110
5.3.3	ASK Specifications	115
6	Foreign Object Detection	117
6.1	Background	117
6.2	Open-air Q-Test (pre-power transfer FOD method).....	117
6.2.1	Introduction.....	117
6.2.2	Movement Timer.....	120
6.2.3	Settling Timer	120
6.2.4	Glossary	120
6.2.5	Open-air Q-Test Specifications.....	120
6.2.6	Theory of Operation.....	121
6.2.7	PRx movement and digital ping	125
6.3	MPP Power Loss Accounting (in-power transfer FOD method)	126
6.3.1	Introduction.....	126
6.3.2	MPLA Specifications	127
6.3.3	MPLA Equations.....	130
6.3.4	Eco-System Scaling	131
6.3.5	Process of Extracting LQK-Dependent Coefficients.....	133
6.3.6	FO power estimation error outside 2x2 cylinder	134
6.3.7	FO Detection Thresholds	135
6.3.8	In-Power FOD Action	138

6.3.9	Accessory Power Loss Requirements	140
6.3.10	Error Budget	140
6.3.11	Measuring coil current	147

7 Annex 149

7.1	PTx Working with Legacy PRx.....	149
7.1.1	Background.....	149
7.2	Mitigation of Saturation for BPP.....	149
7.2.1	System Model	149
7.2.2	SHO Specifications	153
7.3	Loss-Split Modeling: A framework for calculating localized eddy-current losses	153
7.3.1	Introduction.....	153
7.3.2	Comparison between the standard T-Model and Loss-Split Model	155
7.3.3	Determining the Loss-Split Model Parameters	156
7.3.4	Calculating Power Loss using Loss-Split Model	157
7.3.5	Loss-Split Model Validation	158
7.4	Resistive Coupling Factor	158
7.4.1	Introduction.....	158
7.4.2	Definition of Mutual Resistance and K_r	158
7.4.3	Cause of Mutual Resistance	159
7.4.4	Why is K_r non-negligible.....	161

IECNORM.COM : Click to view the full PDF of IEC 63563-10:2025

List of Figures

Figure 2.1.3 : 1 Multipole magnet design that tightly couples strong permanent magnetic fields within the region of the magnet array	11
Figure 2.1.3 : 2 Accurate magnetic alignment within a 2mm radius (without case and with silicone case)	11
Figure 2.2.2 : 3 System block diagram	15
Figure 2.2.2 : 4 MPP PTx functional diagram	15
Figure 2.2.2 : 5 MPP accessory functional diagram (e.g., PRx case, wallet, automotive dash-mount)	15
Figure 2.2.2 : 6 MPP PRx functional diagram	16
Figure 4.2.1.1 : 7 Exploded view of PTx coil system model	20
Figure 4.2.1.3 : 8 Exploded view of the Coil Module for the PTx Coil System Model	21
Figure 4.2.1.3 : 9 Side view of PTx Coil Module	22
Figure 4.2.1.3 : 10 Top view of PTx ferrite	22
Figure 4.2.1.4 : 11 Magnet Array top view	24
Figure 4.2.1.5 : 12 Magnet assembly (Cross-section)	26
Figure 4.2.1.6 : 13 Side view of Bottom Enclosure	27
Figure 4.2.1.8 : 14 Side view of PTx coil system model assembly	29
Figure 4.2.1.9.1 : 15 Transmitter orientation magnets (Top View)	30
Figure 4.2.1.9.1 : 16 Transmitter Orientation Magnet Dimensions and Polarity	31
Figure 4.3.1.1 : 17 Exploded view of PRx coil system model	34
Figure 4.3.1.4 : 18 Exploded view of the coil module for the PRx coil system model	35
Figure 4.3.1.4 : 19 Cross-section of the coil module for the PRx coil system model	36
Figure 4.3.1.4 : 20 Cross-sectional view of coil for the PRx coil system model	36
Figure 4.3.1.4 : 21 Top view of PRx coil system model	37
Figure 4.3.1.5 : 22 Magnet of the PRx coil system model (top view)	40
Figure 4.3.1.5 : 23 Magnet of the PRx coil system model (side view)	40
Figure 4.3.1.5 : 24 Magnetic field of the PRx coil system model	41
Figure 4.3.1.5 : 25 Orientation magnet of the PRx coil system model (side view)	41
Figure 4.3.1.7 : 26 Cross-sectional view showing assembly of PRx coil system model	41
Figure 5.1.3.1 : 27 MPP minimum power delivery requirement shall be $P_I \geq 15W$ for $0mm \leq z \leq 2mm$, $0mm \leq r \leq 2mm$	57
Figure 5.1.3.1 : 28 An MPP PTx shall be able to deliver $P_I \geq 5W$ to an BPP system model PRx for $0mm \leq z \leq 3mm$, $0mm \leq r \leq 8mm$	58
Figure 5.1.3.1 : 29 Cross section view of the system model indicating the "z" gap	58
Figure 5.2.1.1 : 30 System model PRx circuit topology (with BPP and MPP compatibility)	59
Figure 5.2.1.3.1 : 31 Cantilever Equivalent Circuit	60
Figure 5.2.1.3.2.1 : 32 Efficiency vs Crx: sweep of Crx at the maximum coupling position in the system model shows that efficiency is low when $C_{rx} < 300nF$ (system is capacitive)	62
Figure 5.2.1.3.2.1 : 33 Bode plot of $Z_{in}(s)$ at maximum coupling location with two different Crx values. With $C_{rx}=60nF$, the system impedance is capacitive, which is undesirable.	63

Figure 5.2.1.3.2.1 : 34 Bode plot of $G(s)$ at maximum coupling location with two different C_{rx} values. $C_{rx}=710\text{nF}$ has ~1.4dB higher gain than $C_{rx}=60\text{nF}$.	63
Figure 5.2.1.5 : 35 System model PR_x V_{rect}/I_{rect} profile	65
Figure 5.3.1 : 36 PTx power stage block diagram	66
Figure 5.3.1.1 : 37 Definition of inverter phase θ	66
Figure 5.6.1 : 38 MPP Power Negotiation Flow	70
Figure 5.6.1 : 39 Top-level diagram	72
Figure 5.6.1 : 40 Digital Ping Flowchart	73
Figure 5.6.1 : 41 Identification 128kHz Flowchart	74
Figure 5.6.1 : 42 Identification 360kHz Flowchart	75
Figure 5.6.1 : 43 Configuration Flowchart	76
Figure 5.7.1.2.1 : 44 E0 and E1 Fit Example	80
Figure 5.7.1.2.1 : 45 Kest E0 and E1 Extraction Flow	80
Figure 5.7.1.4 : 46 Example PTx/PRx Kest Error Stack-up	82
Figure 5.8.1.1 : 47 Typical Output Impedance Plot (V_{rect} vs I_{rect})	84
Figure 5.8.1.2.1 : 48 V_{rect} timing diagram during load step procedure in the system model	85
Figure 5.8.1.2.2 : 49 V_{rect} timing diagram during load dump procedure in the system model	85
Figure 5.9.2.3.1 : 50 Set Pr_max Overall Flow	88
Figure 5.9.2.3.1 : 51 Example Time Sequence	89
Figure 5.9.2.3.2 : 52 Gain Measurement Flow	90
Figure 5.9.2.3.3 : 53 Set initial V_{rect_target} and Pr_max based on $G1 \cdot G2$	91
Figure 5.9.2.3.3 : 54 Pr_max vs $G1 \cdot G2$	91
Figure 5.10.2.2.1 : 55 Tx Voltage Control Flow Chart	95
Figure 5.10.2.3.3 : 56 Ilim control diagram	97
Figure 5.11.1.0.1 : 57 V_{rect} vs inverter phase at light load	101
Figure 5.11.1.0.1 : 58 Output impedance with 50 and 120 degrees inverter phase	102
Figure 5.11.1.0.2 : 59 Gain (V_{rect}/V_{in}) with and without C_d	102
Figure 5.11.1.0.2 : 60 Load release from 7W to 0W, with and without C_d , and with mitigations implemented in the system model	103
Figure 5.11.1.0.3 : 61 ZVS state with and without C_d , and with mitigations implemented in the system model	103
Figure 6.1 : 62 MPP Comms Physical System Model	105
Figure 6.2.1.1 : 63 System Model for FSK Transmitter	106
Figure 6.2.1.2 : 64 System Model for FSK Receiver	107
Figure 6.2.1.2 : 65 Sample Waveform: Digital Ping 360 kHz AC2 node voltage	108
Figure 6.3.1 : 66 (a) Primary Resonant Capacitor Amplitude and (b) Primary Resonant Capacitor Phase Shift	110
Figure 6.3.2.1 : 67 System Model for ASK Modulator at 128 kHz	111
Figure 6.3.2.1 : 68 System Model for ASK Modulator at 360 kHz	112
Figure 6.3.2.1 : 69 Representative Waveforms for ASK Modulator at 360 kHz	112
Figure 6.3.2.2 : 70 System Model for ASK Receiver	113
Figure 6.3.2.3 : 71 ASK Modulation Trends for (a) DC Load Current and (b) Capacitor Modulation	114

Figure 7.2.1 : 72 Detection Capability V.S. Thermal Requirements .	118
Figure 7.2.1 : 73 Simplified flow diagram for open-air Q test	119
Figure 7.2.6.1 : 74 Implementation of how to measure ring response	121
Figure 7.2.6.1.0.1 : 75 bias ping configuration	122
Figure 7.2.6.4.2 : 76 PRx replaced before the movement timer expires to prevent false fo flag	124
Figure 7.2.7 : 77 Example of q-deflection profile when Prx is approaching ptx	126
Figure 7.3.4.2 : 78 Eco-System Scaling Diagram	133
Figure 7.3.5 : 79 Linear fit error for coil and friendly metal losses. The resistances Rtx and Rrx represent the free-air coil resistances at the switching frequency.	134
Figure 7.3.6 : 80 MPLA estimation error for P_FO grows monotonically away from origin.	135
Figure 7.3.7.2 : 81 15W PFO error distribution with and without FO at 85° critical heating radius (scenario 2: Q-test does detect no FO)	137
Figure 7.3.7.2 : 82 10W PFO error distribution with and without FO at 70° critical heating radius (scenario 1: Q-test detects FO)	137
Figure 7.3.8.1 : 83 Recommended flowchart for PTx FOD action.	139
Figure 7.3.10.3 : 84 PRx Compliance Test pFO Distribution	145
Figure 7.3.10.5 : 85 Compliance Test Ppr shift explanation for Scenario 2 (15W)	147
Figure 8.2.1.1 : 86 Comparison of PTx current with and without SHO	150
Figure 8.2.1.2 : 87 System Model SHO detection flowchart	151
Figure 8.2.1.3 : 88 System Model SHO mitigation flowchart	152
Figure 8.3.1 : 89 Simulation based power accounting flow	154
Figure 8.3.1 : 90 Loss-Split Power Accounting Flow	154
Figure 8.3.2 : 91 Standard T-Model	155
Figure 8.3.2 : 92 Loss-Split T-Model	155
Figure 8.4.2 : 93 Mutual Resistance Model at a Single Frequency	159
Figure 8.4.3.2 : 94 Non-linear B-H curve introduces phase offset between PTx current and the integral of PRx induced voltage, where the out-of-phase component is captured by mutual resistance	161
Figure 8.4.4 : 95 Example values of Kr measured with a mated MPP PTx/PRx coil sample	162

List of Tables

Table 4.2.1.3 : 1 Mechanical dimensions for the coil module of the PTx coil system model	23
Table 4.2.1.5 : 2 Magnetic field specifications for magnet array	26
Table 4.2.1.7 : 3 Mechanical dimensions for the bottom enclosure of the PTx coil system model	28
Table 4.2.1.8 : 4 Assembly dimensions of PTx coil system model	29
Table 4.2.1.9.1 : 5 Flux density at 0.85mm from PTx orientation magnet surface	31
Table 4.2.2.1 : 6 Electrical Parameters of the PTx Coil System Model in Free-Air	32
Table 4.3.1.4 : 7 Assembly specifications of coil module for the PRx coil system model	36
Table 4.3.1.4 : 8 Mechanical specifications of the PRx coil system model	38
Table 4.3.1.5 : 9 Magnet properties of the PRx coil system model	39
Table 4.3.1.7 : 10 Assembly specifications for the PRx coil system model	42
Table 4.3.1.7 : 11 Mechanical dimensions of support plate	42
Table 4.3.2.1 : 12 Electrical Parameters of the PRx Coil System Model in Free-Air	42
Table 4.4.1 : 13 Mated electrical parameters (Test case: $r=0$, $z=0$ mm)	43
Table 4.4.1 : 14 Mated electrical parameters (Test case: $r=2$, $z=2$ mm)	43
Table 5.2.1.1 : 15 PRx series tuning configuration	59
Table 5.2.1.4 : 16 PRx electrical properties (system model)	64
Table 5.3.1.2 : 17 PTx power stage capacitor switches configuration	67
Table 5.3.1.3 : 18 PTx electrical properties (system model), during power transfer	67
Table 6.3.2.1 : 19 Selection of MOD_BASE	111
Table 7.2.4 : 20 Glossary	120
Table 7.3.2.3 : 21 Eco-System Parameter Representation	130
Table 7.3.4.1 : 22 Eco-System scaling terms exchanged between PTx and PRx at startup	131
Table 7.3.7.1 : 23 MPLA Scenarios	136
Table 7.3.10.2 : 24 Measurement Error Calculation for Scenario 1 (10W) and Scenario 2 (15W)	143
Table 7.3.10.3 : 25 pFO Error Budget Calculation	144

1 General Description

1.1 Introduction

1.1.1 Scope

This specification defines MPP (Magnetic Power Profile), an extension to Qi v1.3 BPP (Baseline Power Profile). Manufacturers can use this specification to implement PTx and/or PRx that are interoperable.

1.1.2 Document organization

The MPP (Magnetic Power Profile) Specification is organized as these documents:

1. MPP System Specification (this document)
2. MPP Communications Protocol Specification

MPP is an extension of the Baseline Power Profile (BPP) and utilizes some (but not all) features defined in the Extended Power Profile (EPP). Where relevant, refer to the Qi v2.0 Specification.

1.1.3 Design goals

Magnetic Power Profile (MPP) is an interface which allows for:

- Never missing the sweet spot - ease of attach through ring of magnets
- Ecosystem of powered and unpowered accessories
- Conveniently using your device while charging
- Delivering high power (15W) safely
- Preventing interference with vehicle key fobs without regulatory issues by operating at 360 kHz
- Compatibility with Qi 2.0 BPP products and maintaining near-parity backward compatibility with Qi 1.x BPP products

Sweet spot

The goal for MPP is to enable a new wireless charging experience for users where they will never miss the charging "sweet spot" and can consistently, efficiently, and safely charge their devices at high power. To achieve accurate alignment between the PTx and PRx coils, a circular array of magnets has been added that surround the coils. The magnetic alignment provides tactile feedback to the user guiding accurate placement even in the case where the user isn't directly looking at the PTx. Conveniently, the magnetic attachment enables users to use their device while it is charging and greatly simplifies docking functionality.

Magnet array

The magnet array has been carefully designed so that it can coexist with the wireless power transfer system to deliver high power transfer at high efficiency. Figure 2.1.3: 1 shows the multipole magnet design that tightly couples strong permanent magnetic fields within the region of the magnet array, keeping most of the strong fields away from the magnetic shielding material of the power transfer coils.

Because of the consistent accurate alignment, the magnetic state-space that the system must be designed to work across is reduced. Figure 2.1.3: 2 shows data from a study where 99.9% of placements aligned the PTx and PRx within a 2mm radius

¹. By reducing the state-space, the design of features like foreign object detection is simplified.

¹ The placement study used a case with integrated magnets as shown in Figure 2.1.3: 1

Benefits

The benefits of MPP also extend further than just wireless charging: it enables an ecosystem of powered and unpowered accessories. Because of the convenience of magnetic attach, it is expected that a new category of portable charging products will arise, and with this in mind, MPP has been designed to ensure that charging at 360 kHz will not cause interference with vehicle key fobs. All these benefits and experiences have been enabled in MPP while also being compatible with Qi 2.0 BPP and having nearly 100% backwards compatibility with Qi 1.x BPP.

Figure 2.1.3: 1 Multipole magnet design that tightly couples strong permanent magnetic fields within the region of the magnet array .

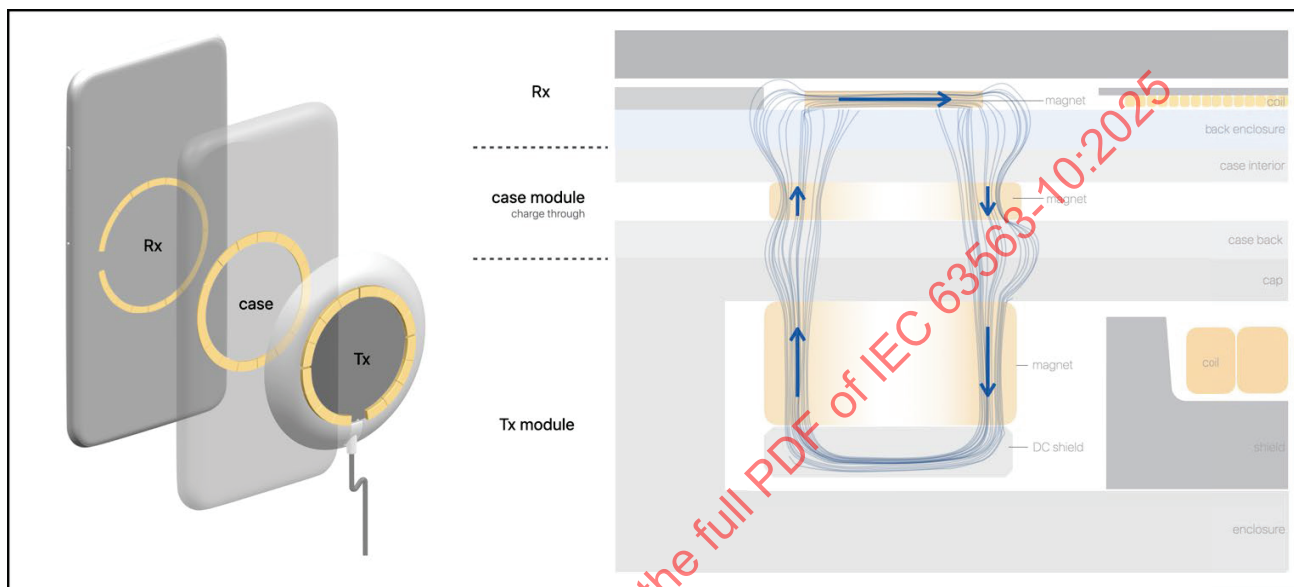
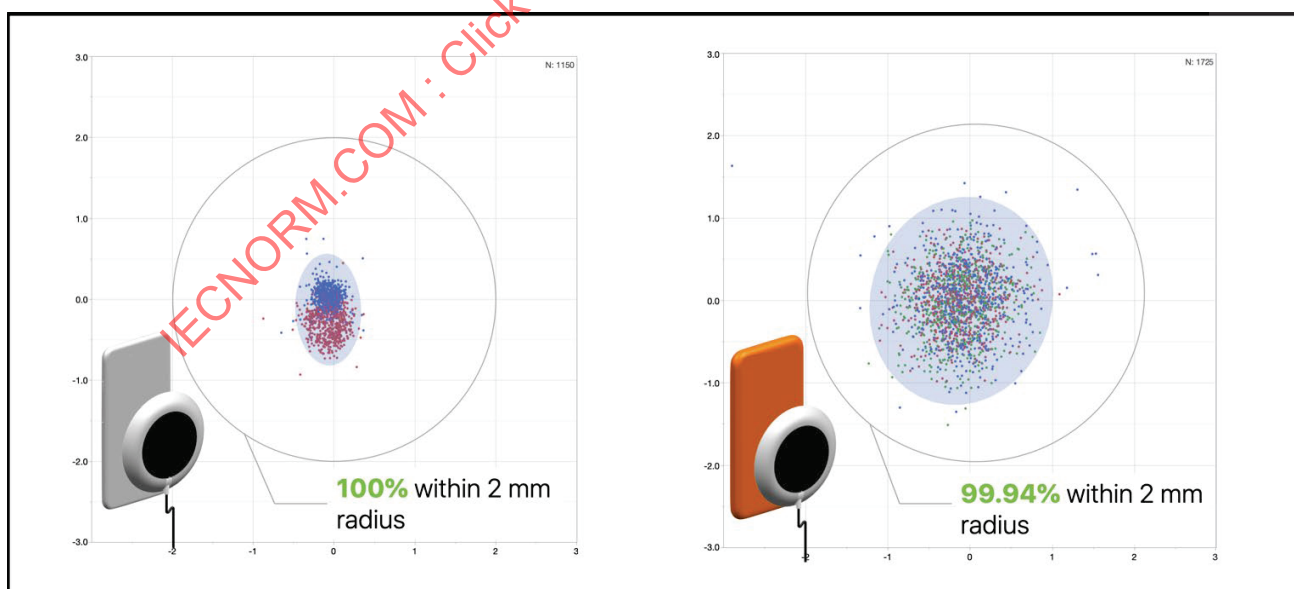


Figure 2.1.3: 2 Accurate magnetic alignment within a 2mm radius (without case and with silicone case).



1.1.4 BPP and MPP interoperability

Backward compatibility with PRx or PTx that do not support MPP is achieved by operating in BPP at up to 5 W:

- MPP PTx support operation as a BPP PTx (i.e., 5 W)
- MPP PRx support operation as a BPP PRx (i.e., up to 5 W)

To support both MPP and BPP, the system uses dynamic re-tuning. Dynamic re-tuning is achieved by switching appropriate capacitors in series with the Primary Coil in the PTx, and the Secondary Coil in the PRx.

Compared to BPP, this requires:

- For PTx: two additional capacitor values and two switches (e.g., MOSFETs)
- For PRx: one additional capacitor value and one switch

The magnet array resolves the problem of magnetic flux density in Shielding materials reaching saturation (associated with the deprecated magnetic alignment feature in Reference Designs A1, A5, A9). See § 4.2 PTx Coil System Model and § 4.3 PRx Coil System Model .

The deprecated magnetic alignment feature is described in Qi v1.2.2 Pt 4, Sec 2 Overview:

“NOTE Power Receivers that use thin magnetic Shielding have been found to experience reduced performance on Power Transmitters that contain a permanent magnet in or near the Active Area. Such Power Receivers may exhibit, for example, less positioning freedom and/or a longer charging time. For this reason Power Transmitter designs A1, A5, and A9 have been deprecated as of version 1.2 of the Qi Power Class 0 Specification.”

For BPP PRx that implements Shielding with a low saturation property, the magnet array in an MPP PTx can cause saturation. Such combinations of MPP PTx and BPP PRx can exhibit sub-harmonic oscillation. A solution for this is described in § 8.2 Mitigation of Saturation for BPP .

1.1.5 Related documents

General Documents

- Introduction
- Glossary, Acronyms, and Symbols

System Description Documents

- Mechanical, Thermal, and User Interface
- Power Delivery
- Communications Physical Layer
- Communications Protocol
- MPP Communications Protocol
- Foreign Object Detection
- NFC Tag Protection
- Authentication Protocol

1.2 Architectural overview

1.2.1 System Description

Figure 2.2.2: 3 and Figure 2.2.2: 4 show the MPP system architecture. Some elements are identical to those found in BPP. The system consists of the following blocks:

- External power source - in many cases a separate adapter such as a USB PD brick.
- Variable Voltage Supply - for voltage control of the power signal
- Inverter - a full-bridge DC/AC converter to produce the AC power signal
- Resonant circuit - switched capacitors in series with the coil to boost power transfer capability and to support MPP and BPP modes
- FSK (de-)modulator - enables communication from PTx to PRx using FSK
- ASK (de-)modulator - enables communication from PRx to PTx using ASK
- Rectifier - AC/DC conversion
- Controllable input current power converter - DC/DC converter that controls both its input current (drawn from the rectifier) and output voltage
- External power load - typically a battery and its associated host system e.g., application processor and peripherals

When the MPP system starts up, it will initially operate in Qi BPP frequency band to negotiate and determine whether the PTx and PRx both support MPP.

Power signal frequency

If MPP is supported, the system will restart and operate at a fixed power transfer frequency of 360kHz, which was selected to mitigate interference with nearby vehicle key fobs. This operating frequency is outside of the existing BPP frequency range and therefore requires different tuning capacitors on both the PTx and PRx for high and efficient power transfer. Because of this, both the PTx and PRx features switchable tuning capacitor banks to support both MPP and BPP.

Control of power transfer

To control the magnitude of power transfer, the DC voltage of the inverter is regulated and controlled. Additionally, modulation of the phase shift between the inverter's two half bridges may also be used at light loads. The details relating to power transfer is further discussed in the Power Delivery section.

Communication

To facilitate bidirectional communication, both FSK and ASK are used. On the PTx side, communications to the PRx uses FSK modulation of the power transfer frequency. The PRx side modulates its load to affect ASK communication to the PTx. MPP uses the same authentication scheme as EPP, but to speed up the authentication process, MPP uses fast FSK with 128 cycles per bit of data transferred. § 6 Communications Physical Layer specifies the changes to the physical layer.

Communication protocol

There are many additional features that have been implemented as part of MPP to enhance the user experience such as: free-air ping as pre-power FOD, enhanced power accounting as during-power FOD, thermal cloaking, data streams and new control loops. To enable these features, many changes have been implemented to the communications protocol which take effect after the system has switched into MPP mode. This protocol is in the document "MPP Communications Protocol."

Foreign Object heating

When an electrically conductive or ferromagnetic (with a high coercivity) Foreign Object (FO) is placed into the active area of the wireless power transfer (WPT) system, the AC magnetic field can cause the FO to heat up. If the FO reaches elevated temperatures this can compromise the system or its users. Foreign Object Detection (FOD) methods are implemented to prevent this from happening. MPP supports two FOD methods: open-air ping and MPP power loss accounting (MPLA).

Open-air ping

The open-air ping method takes place before power transfer, and it aims to detect FOs that are on the PTx surface before the PRx is placed. The advantage of this method is that there is no influence or impact by the PRx device, which is outside of the control of the PTx designer. Because this method is only dependent on the PTx, FOD performance can be guaranteed by design for this use case. This method is described in Annex B in the Foreign Object Detection book.

MPP power loss accounting (MPLA)

The second FOD method is applied during power transfer and can detect FOs regardless of when it is introduced into the WPT system. This method uses an enhanced power loss accounting model to estimate the magnitude of power loss that is causing FO heating and can throttle the power transfer magnitude to ensure the power lost in the FO won't cause excessive heating. One key feature of the improved model is the ability for PTx to adapt its model to consider the impact of the PRx on the PTx's losses and vice versa. This is important because the coil design and friendly metal on the PRx can also cause a change to the coil and friendly metal losses on the PTx. By taking this into account the FOD performance can be improved for more PTx and PRx combinations in the ecosystem. This method is described in § 7.3 MPP Power Loss Accounting (in-power transfer FOD method) .

Cloaking

There are several circumstances under which a PRx may want to request that wireless charging be paused or stopped. One common case is when the PRx's battery temperature is too high. Another scenario is at the end of the battery charge cycle where trickle charging is inefficient and it may be more desirable to wait until the PRx is further discharged before continuing charging. The cloaking feature is described in § 5.12 Cloak and in the document MPP Communications Protocol.

Power control

In addition to the (voltage) XCE control loop that is used to control power transfer, the PRx also regulates the current charging its battery. Typically, the battery charger current control loop is slow, but there are cases where the load power can suddenly drop (i.e. "load dump"). This can cause over-voltage on the PRx. To manage this, the battery charger current control loop coordinates with the XCE control loop to avoid over-voltage and other control instabilities. The two control loops are covered in § 5.10 Power Transfer Control .

Coil design

The coil system models and requirements are covered in § 4 Coil Design . This section includes details on the coil winding, shielding, magnet array, orientation magnets and externally observable compliance requirements in terms of magnetic alignment performance and the electrical parameters to enable BPP and MPP compatibility.

The coil system models provide nominal implementation models of an MPP PTx and MPP PRx. These are the basis for deriving externally observable requirements for compliant implementations of MPP PTx and PRx. While the system models provide a starting point for PTx or PRx designs, a compliant implementation may differ internally, if they comply with the externally observable requirements in the specification.

1.2.2 System block diagrams

Figure 2.2.2: 3 shows the system-level diagrams for a typical MPP system. There are also functional diagrams for three sub-blocks:

- MPP PTx: Figure 2.2.2: 4
- MPP accessory: Figure 2.2.2: 5
- MPP PRx: Figure 2.2.2: 6

Figure 2.2.2: 3 System block diagram.



Figure 2.2.2: 4 MPP PTx functional diagram.

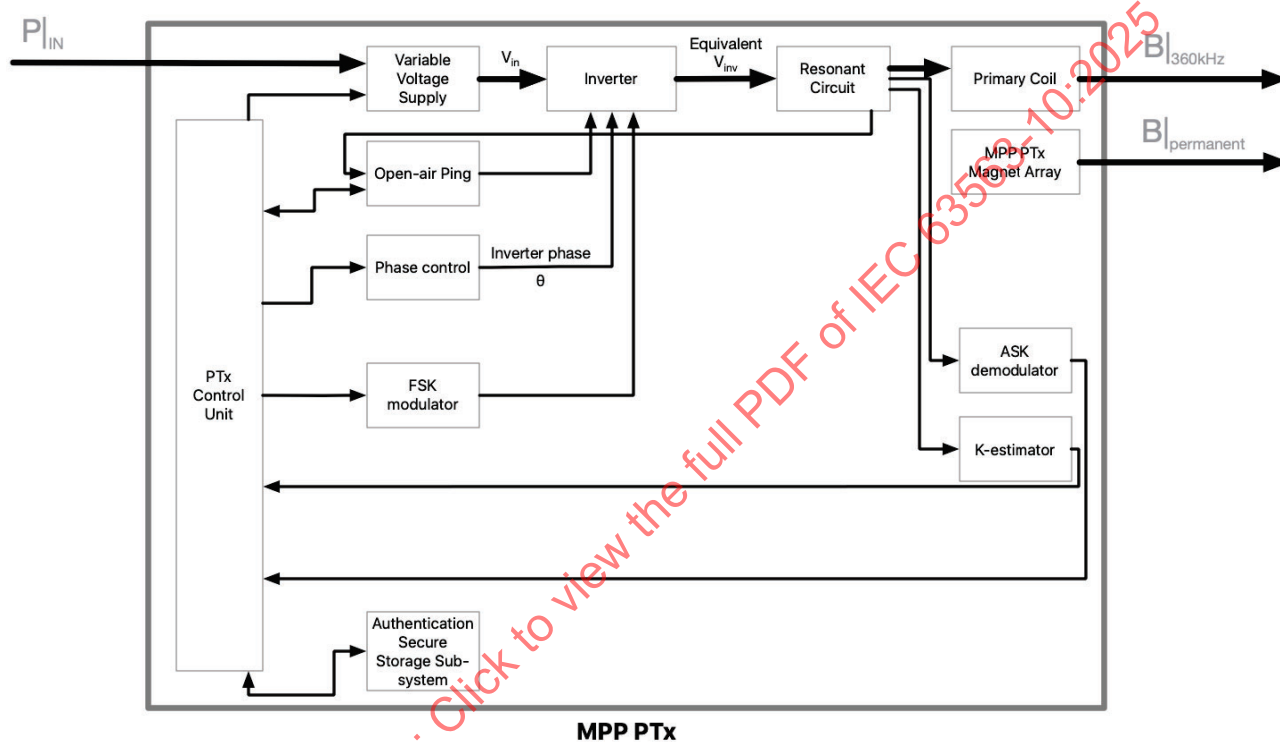
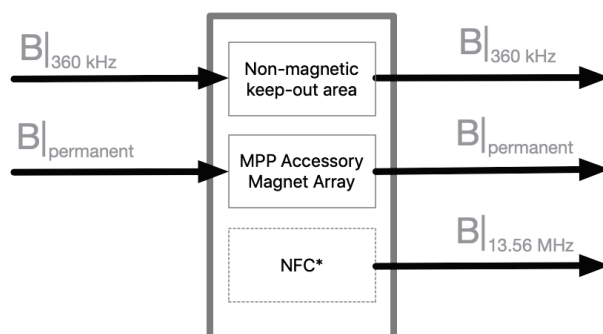
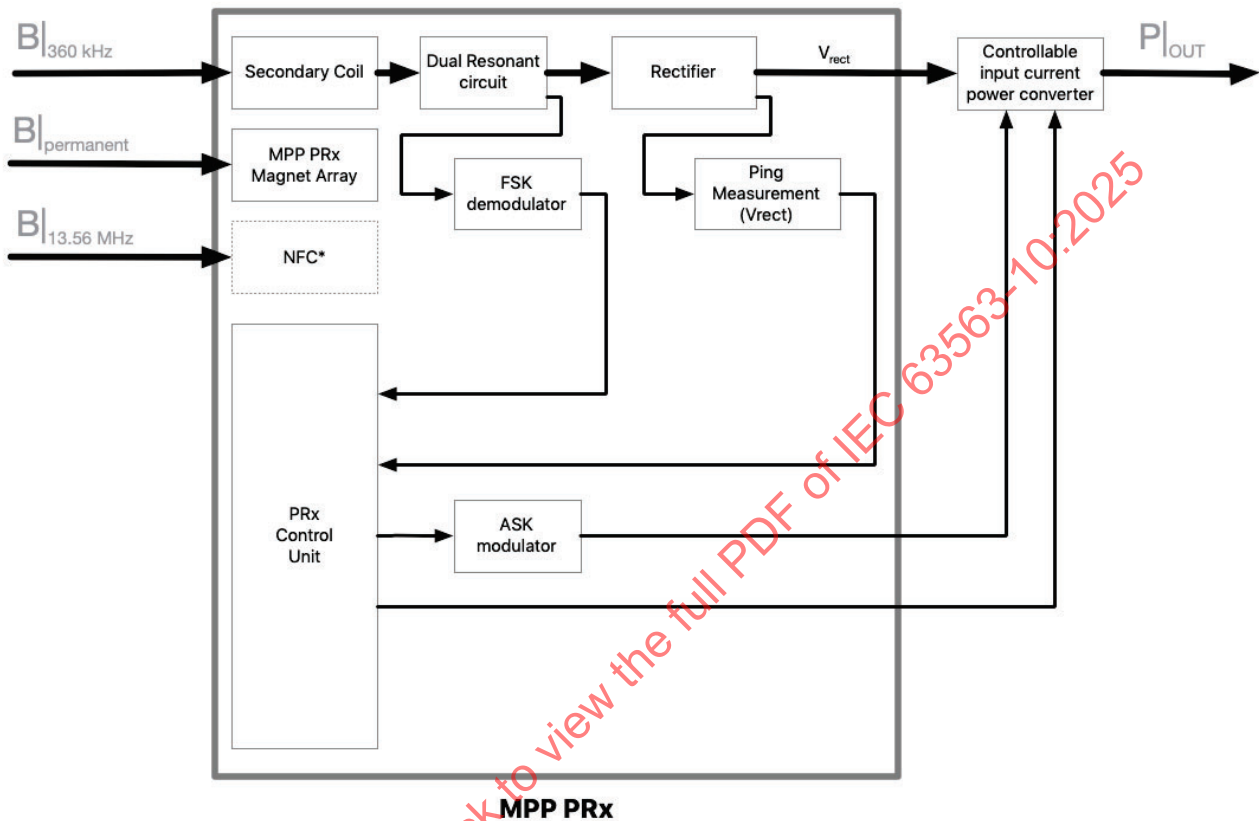


Figure 2.2.2: 5 MPP accessory functional diagram (e.g., PRx case, wallet, automotive dash-mount).



* Independent NFC applications can co-exist with MPP by interrupting power transfer. Same applies to the PTx (not shown in the picture).

Figure 2.2.2: 6 MPP PRx functional diagram.



1.3 Glossary

1.3.1 Definitions

Magnetic Power Profile (MPP): An extension to BPP that features magnets that guarantee tight alignment of the power transmitter and receiver, which enables safe power transfer up to 15W while also mitigating key fob interference

MPP power loss accounting (MPLA): An extension to power loss accounting (used in BPP), that uses a model of the physics of the wireless power system to improve accuracy. It enables the PTx and PRx to take temperature and the impact of friendly metal into account (i.e., compensate for these), with a large ecosystem in mind.

Extended Received Power Packet (PLA): The packet that an MPP PRx sends to an MPP PTx containing the received power and rectified power values

Open-Air Ping: The open-air Q test provides a method for detecting Foreign Objects placed on top of a Power Transmitter Product before a Power Receiver Product is brought into the Operating Volume. Refer to Annex B in the Foreign Object Detection book for further detail.

Sub Harmonic Oscillation (SHO): Oscillation at a sub-harmonic frequency of the operating frequency induced by saturation of the PRx ferrite.

System Model: A theoretical nominal implementation which functions as the basis for deriving requirements of compliant MPP PTx and PRx implementations.

2x2 cylinder: A cylinder with a radius of 2mm and a height of 2mm, from the center of the PTx coil. This cylinder is the magnet attach state-space and is used in Figure 4.3.2.1: 27 to define the 15W power delivery region. See § 5.1.3.1 for the definition of z and r used for this cylinder.

1.3.2 Acronyms

Term	Meaning	Comment
PTx	Power Transmitter	
PRx	Power Receiver	
TPT	Test Power Transmitter	
TPR	Test Power Receiver	

1.3.3 Symbols

Symbol	Name	Comment
V _{in}	PTx Inverter Input DC Voltage	
f _{op}	PTx Inverter Switching Frequency	
D	PTx Inverter Duty Ratio	
θ	PTx Inverter Phase Shift	θ=0° means the full-bridge inverter is operating in complementary mode. See § 5.3.1.1 Definition of inverter phase θ
V _{inv}	PTx Equivalent Inverter Voltage	Equivalent inverter voltage that considers the inverter phase shift and duty cycle. See § 5.9.4.1
V _{rect}	PRx rectified DC output voltage	
L _{TX} and L' _{TX}	The inductance of PTx coil module when it's in open air (L _{TX}) or when it's mated with a PRx (L' _{TX})	
L _{RX} and L' _{RX}	The inductance of PRx coil module when it's in open air (L _{RX}) or when it's mated with a PTx (L' _{RX})	
R _{TX} and R' _{TX}	The resistance of PTx coil module when it's in open air (R _{TX}) or when it's mated with a PRx (R' _{TX})	
R _{RX} and R' _{RX}	The resistance of PRx coil module when it's in open air (R _{RX}) or when it's mated with a PTx (R' _{RX})	

K_i	Inductive coupling factor	It's an unitless quantity between 0 and 1. Mutual inductance then is equal to $K_i \sqrt{L_{TX} L_{RX}}$
K_r	Resistive coupling factor	See § 8.4 Resistive Coupling Factor for the definition of K_r and explanation of why it's needed

1.4 System Model vs Spec

In the rest of the MPP System Spec book, we will go through different subsystems that together ensure a safe and efficient power delivery experience in MPP.

In general, most sections include the following subsections:

- System Model: this subsection describes the system model design for this subsystem. It is not required but can be used as a reference design.
- Specifications: this subsection (or a set of subsections) includes the specifications that MPP device shall meet.

Some sections only have the system model description but no specs. This indicates that the corresponding subsystem is not required (but recommended).

IECNORM.COM : Click to view the full PDF of IEC 63563-10:2025

2 Authentication Protocol

2.1 Authentication

Introduction

An MPP PTx shall implement Authentication to provide tamper-resistant identity of its:

- Qi certification (Qi ID number).
- Manufacturer name (PTMC value).

Specifications

Refer to the books "Qi v2.0 Authentication Protocol" and "MPP Communications Protocol".

IECNORM.COM : Click to view the full PDF of IEC 63563-10:2025

3 Coil Design

3.1 Introduction and Background

This section describes the MPP Tx and Rx coil system models.

The coil system models are nominal designs from which the MPP specifications are derived.

It is recommended that MPP PTx or PRx implementations follow these coil system models as closely as possible to minimize the differences with the TPT#MPP1-coil and TPR#MPP1-coil compliance test tools.

Each of the coil system model sub-sections are split into two sections:

- Mechanical specification of the individual components, full assembly, and materials.
- Nominal electrical parameters in free-air and mated conditions.

The final sub-section specifies the coil requirements for PTx and PRx implementations.

3.2 PTx Coil System Model

3.2.1 Mechanical Construction

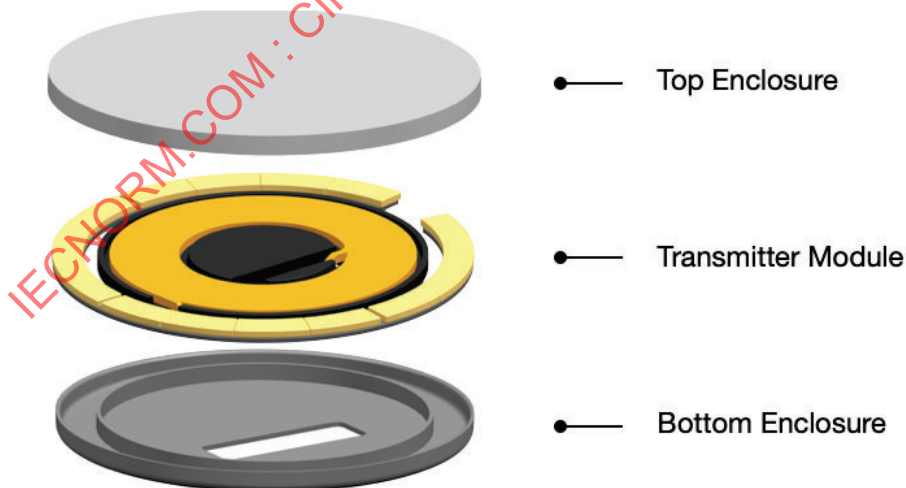
3.2.1.1 Overview

The overall design of the PTx coil system model is shown in Figure 4.2.1.1: 7.

It consists of three main components:

- a top enclosure that defines the interface surface
- a coil module
- a bottom enclosure

Figure 4.2.1.1: 7 Exploded view of PTx coil system model.



3.2.1.2 Top Enclosure

The top enclosure is constructed with plastic.

3.2.1.3 Coil Module (AC magnetics)

The exploded view of the coil module for the PTx coil system model is shown in Figure 4.2.1.3: 8 . The coil module consists of four components:

- circular wound coil
- ferrite shield
- magnet ring
- permeable magnet shunt

The side view of the coil module is shown in Figure 4.2.1.3: 9 .

The coil is 11 turns constructed with Type-1 Litz wire with each turn consisting of 65 strands of individually insulated 80µm diameter copper wire.

The magnetic shielding in the coil module is constructed using DMR95 ferrite.

The purpose of the magnets is to ensure tighter alignment between the transmitter and receiver coils.

Practically, a cutout in the PTx ferrite is needed to allow the external routing of the coil leads. In Figure 4.2.1.3: 10 , the implementation of the ferrite cutout in the system model is shown.

Key mechanical dimensions of the coil module are in Table 4.2.1.3: 1 .

Figure 4.2.1.3: 8 Exploded view of the Coil Module for the PTx Coil System Model.

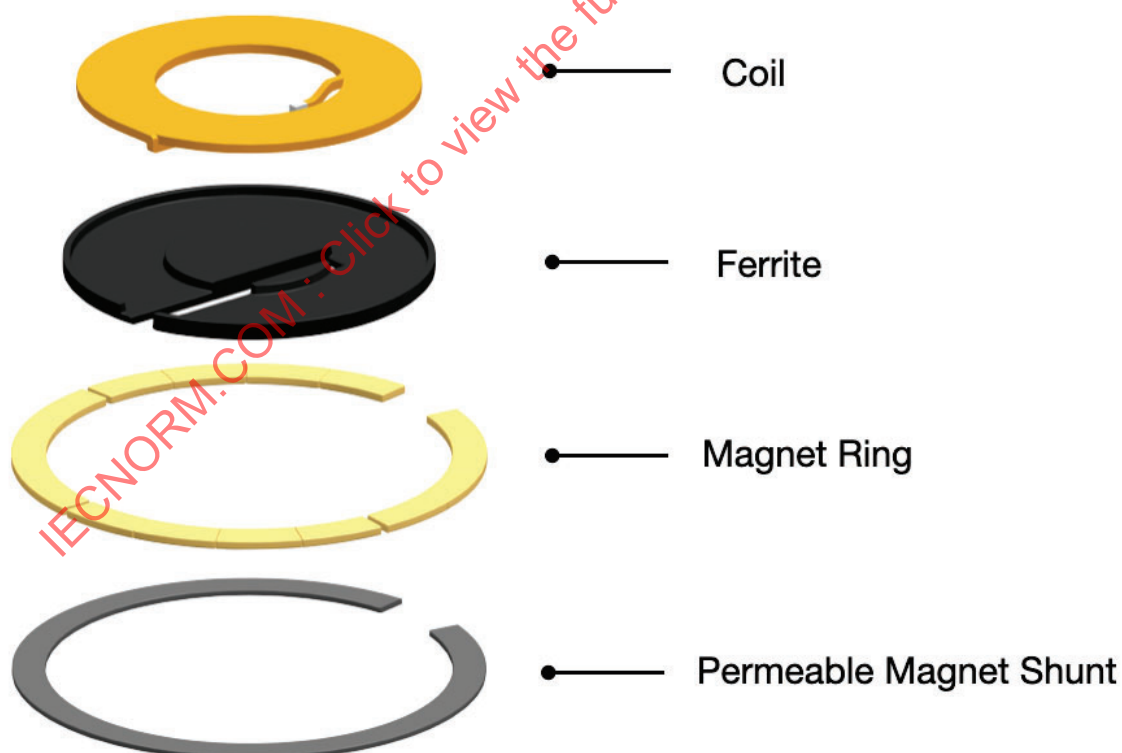


Figure 4.2.1.3: 9 Side view of PTx Coil Module.

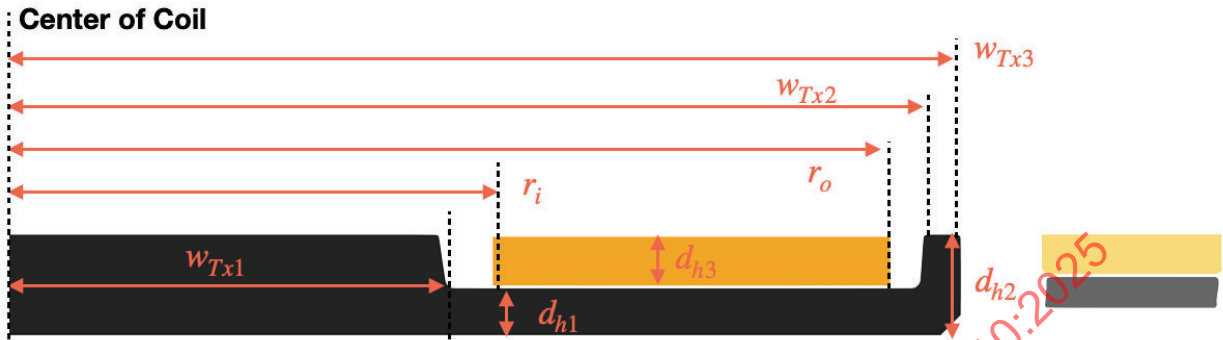


Figure 4.2.1.3: 10 Top view of PTx ferrite.

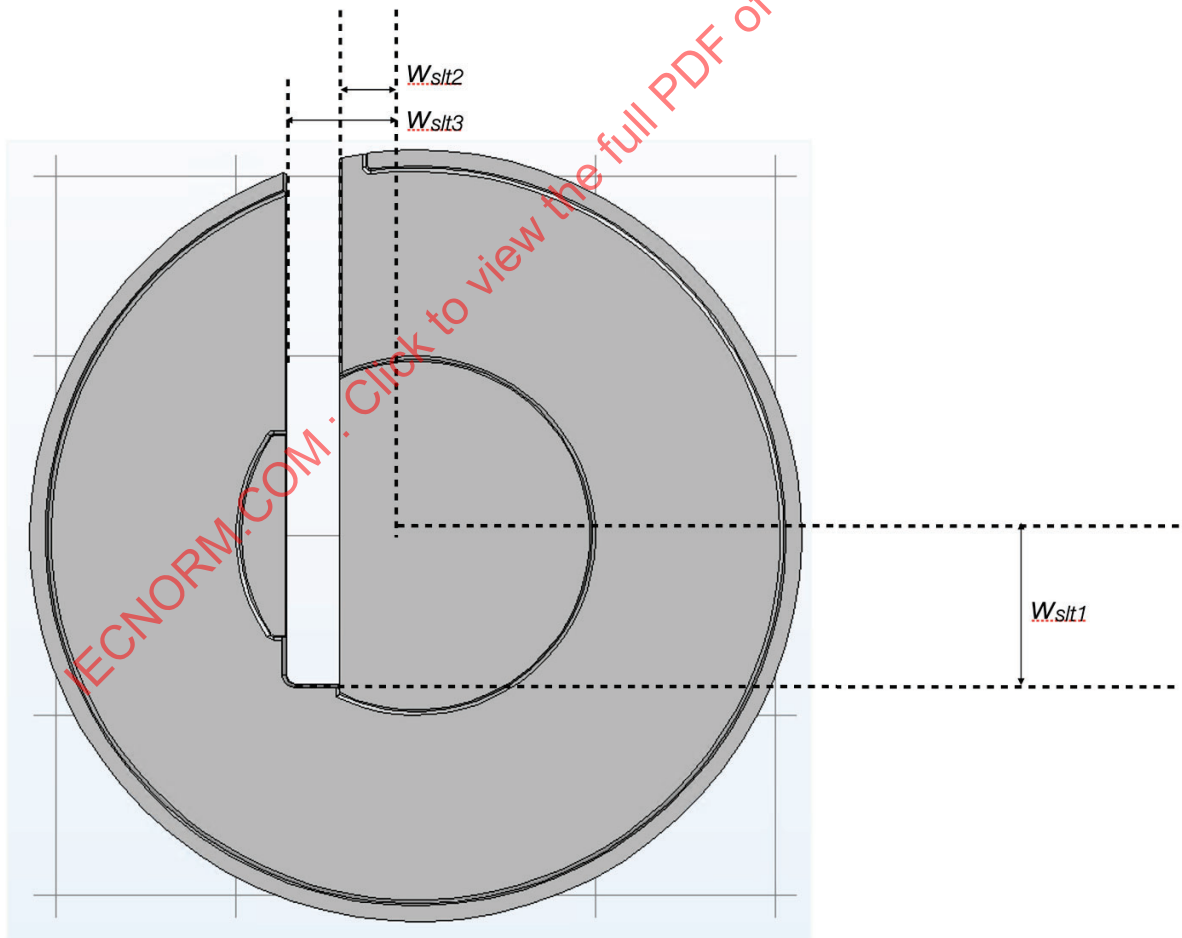


Table 4.2.1.3: 1 Mechanical dimensions for the coil module of the PTx coil system model.

	Description	Nominal Value
r_i	Inner radius of transmitter coil	10.73 mm
r_o	Outer radius of transmitter coil	19.65 mm
w_{Tx1}	Radius of ferrite center post	9.58 mm
w_{Tx2}	Inner radius of ferrite outer post	20.33 mm
w_{Tx3}	Outer radius of ferrite outer post	21.20 mm
d_{h1}	Thickness of ferrite base	1.15 mm
d_{h2}	Overall thickness of ferrite	2.15 mm
d_{h3}	Thickness of transmitter coil	1.03 mm
w_{sl1}	Vertical offset of ferrite cutout slot	8.20 mm
w_{sl2}	Horizontal offset of ferrite cutout slot	4.18 mm
w_{sl3}	Horizontal offset of outside edge of ferrite cutout slot	7.16mm

3.2.1.4 Coil Module (permanent magnets)

The magnet module consists of a permeable magnet shunt and magnets arranged in a circle around the coil module.

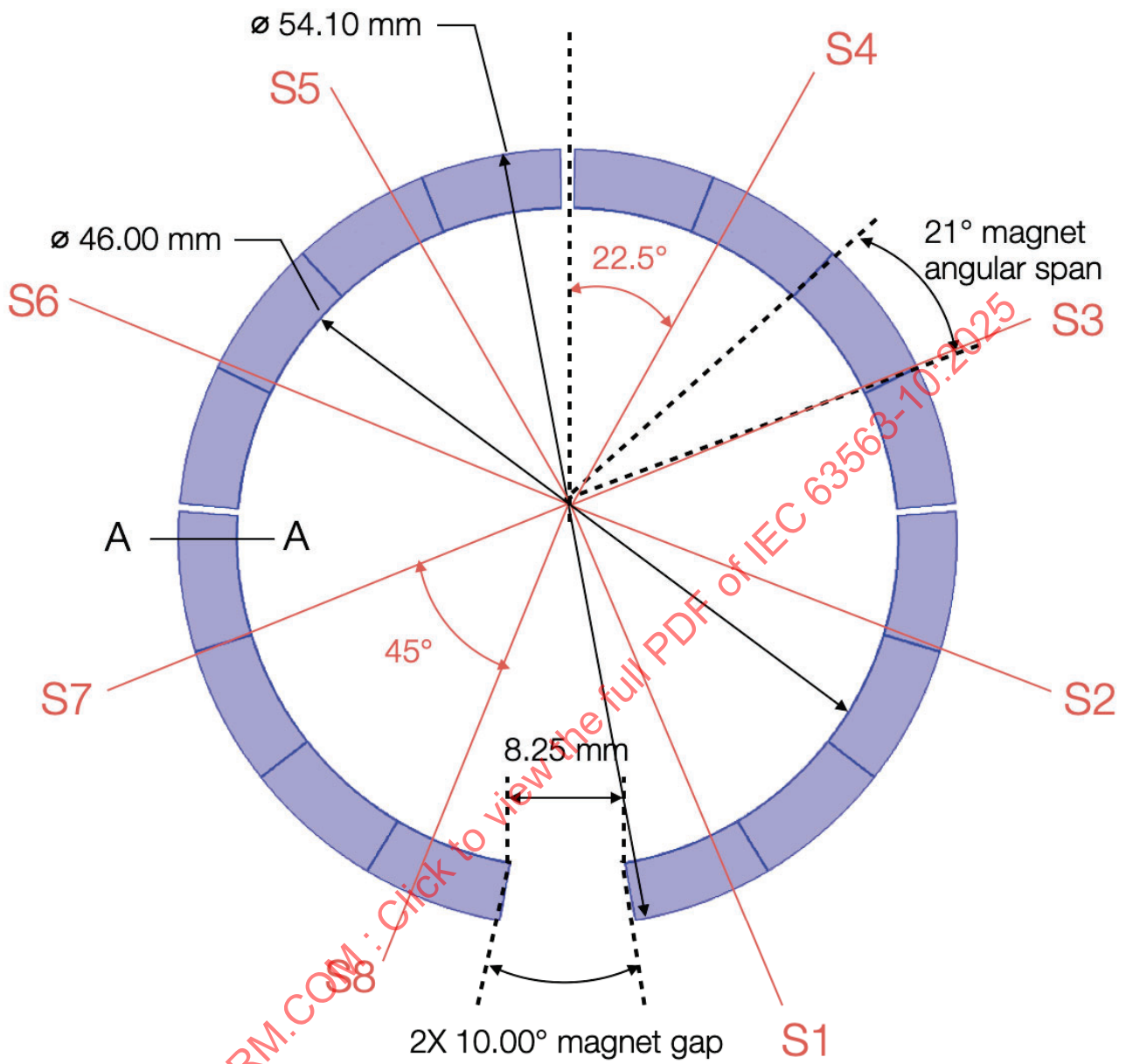
Details of the permanent magnet and shunt dimensions (shown in top view and cross-section view) are illustrated in Figure 4.2.1.4: 11 , § 4.2.1.5 Magnet shunt top view and Figure 4.2.1.5: 12 .

The dimensions and orientation (North or South) of the four poles in each magnet array element are essential for minimizing the impact on the AC magnetics. For the PTx system model, the B-field are measured in z- and xy-directions on the interface surface along S1-S8 as defined in Figure 4.2.1.4: 11 . The values of B-field thus measured are provided in Table 4.2.1.5: 2 .

The magnet array is constructed using NdFeB N48H grade magnets. The magnet array has a Ni-Cu-Ni plating layer of 10µm. The permeable magnet shunt is constructed with DT4. The material is chosen for high saturation flux density and high permeability. The key magnetic parameters of these materials are given here.

Component	Material parameter	Typical values
Magnet array	Br	1.39 T
	Hcb	$> 1.054 \times 10^6$ A/m
	Hcj	$> 1.353 \times 10^6$ A/m
	BHmax	3.7×10^5 T•A/m
Permeable shunt	Bsat	> 2.0 T

Figure 4.2.1.4: 11 Magnet Array top view.



3.2.1.5 Magnet shunt top view

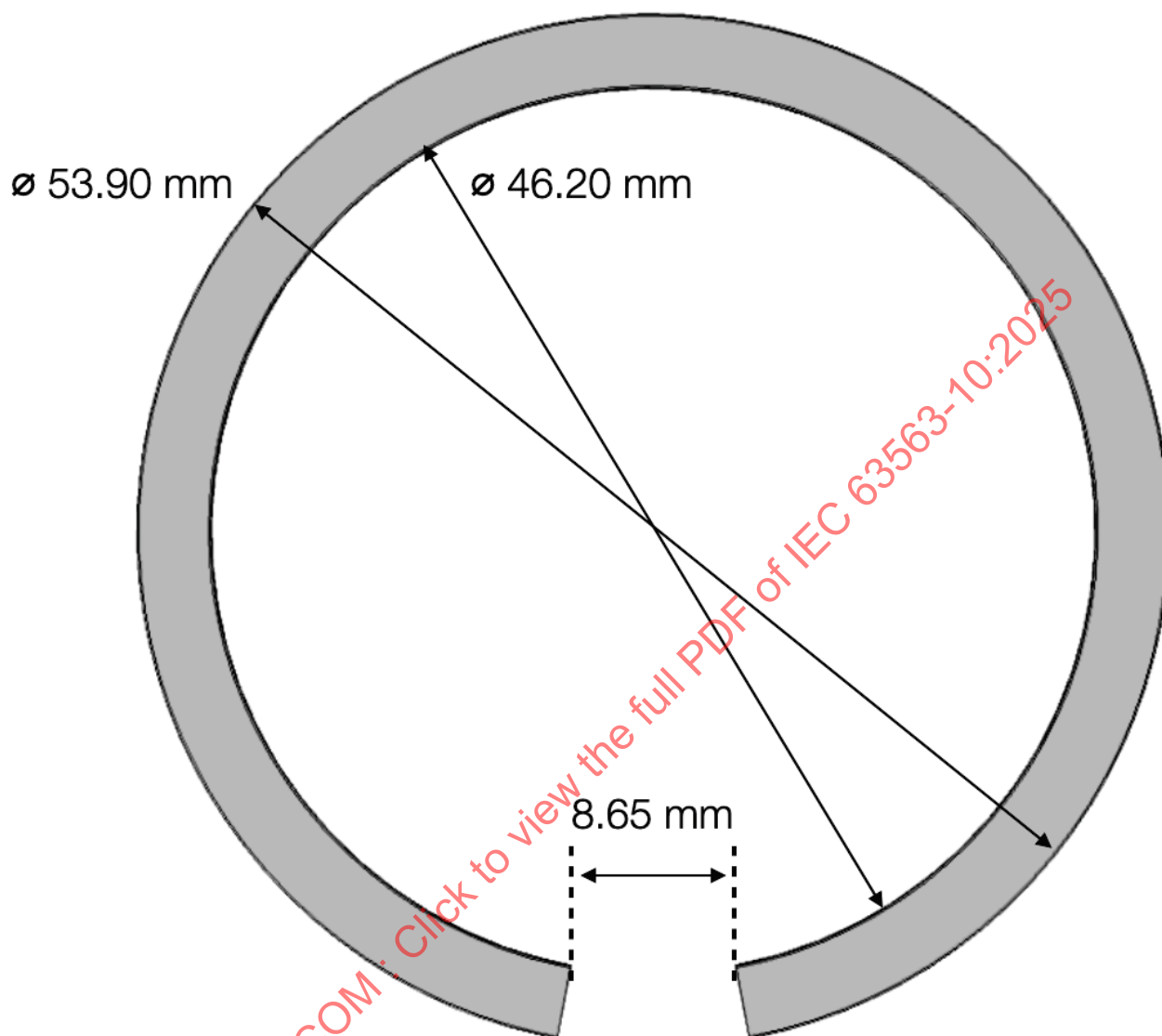


Figure 4.2.1.5: 12 Magnet assembly (Cross-section).

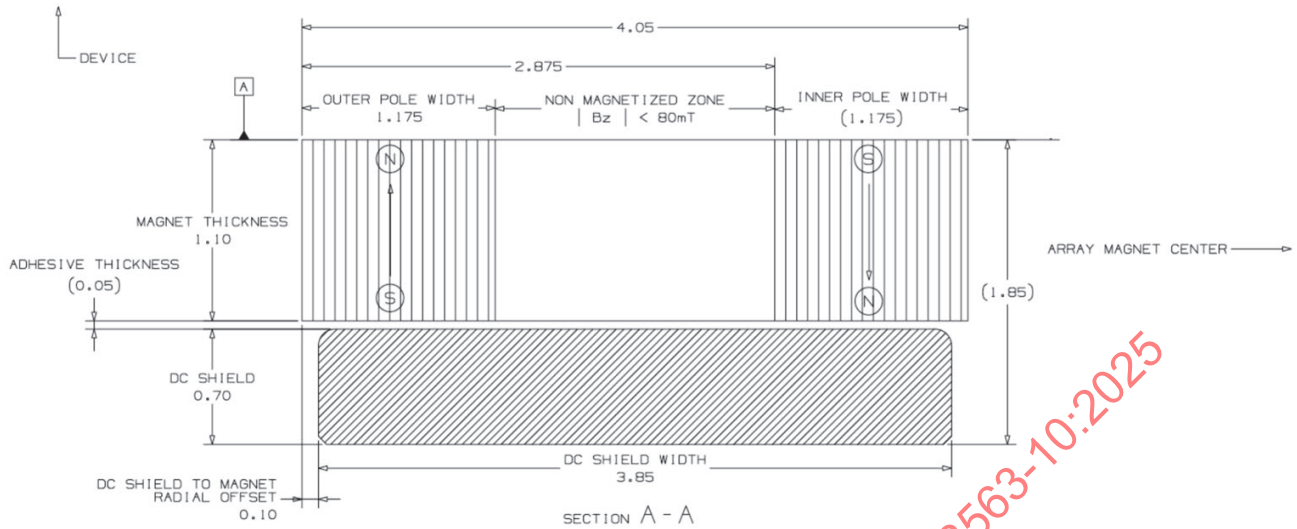


Table 4.2.1.5: 2 Magnetic field specifications for magnet array.

Radial Position (mm)	Bz (T)	Bxy (T)
$r < 19.5$	0	0.025
$19.5 < r < 23$	N/A	0.075
$23 < r < 24$	-0.185	N/A
$24.5 < r < 25.5$	N/A	0.1925
$26 < r < 27$	0.185	N/A
$27 < r < 30$	N/A	0.075
$r > 30$	0	0.025

* The $z=0$ plane refers to the interface surface, and $r=0$ refers to the center of the magnetic array.

3.2.1.6 Bottom enclosure

The bottom enclosure is made from 6061 grade aluminum. A cut-out is added to the bottom enclosure. This cutout is aligned with the ferrite cutout shown in Figure 4.2.1.3: 10 . This is to expose the coil leads and allow connection to external circuit. The dimension of the cutout is shown in § 4.2.1.7 Top view of bottom enclosure .

The cross-sectional and top view of the bottom enclosure is shown in Figure 4.2.1.6: 13 .

Mechanical dimensions of the bottom enclosure are specified in Table 4.2.1.7: 3

Figure 4.2.1.6: 13 Side view of Bottom Enclosure.



IECNORM.COM : Click to view the full PDF of IEC 63563-10:2025

3.2.1.7 Top view of bottom enclosure

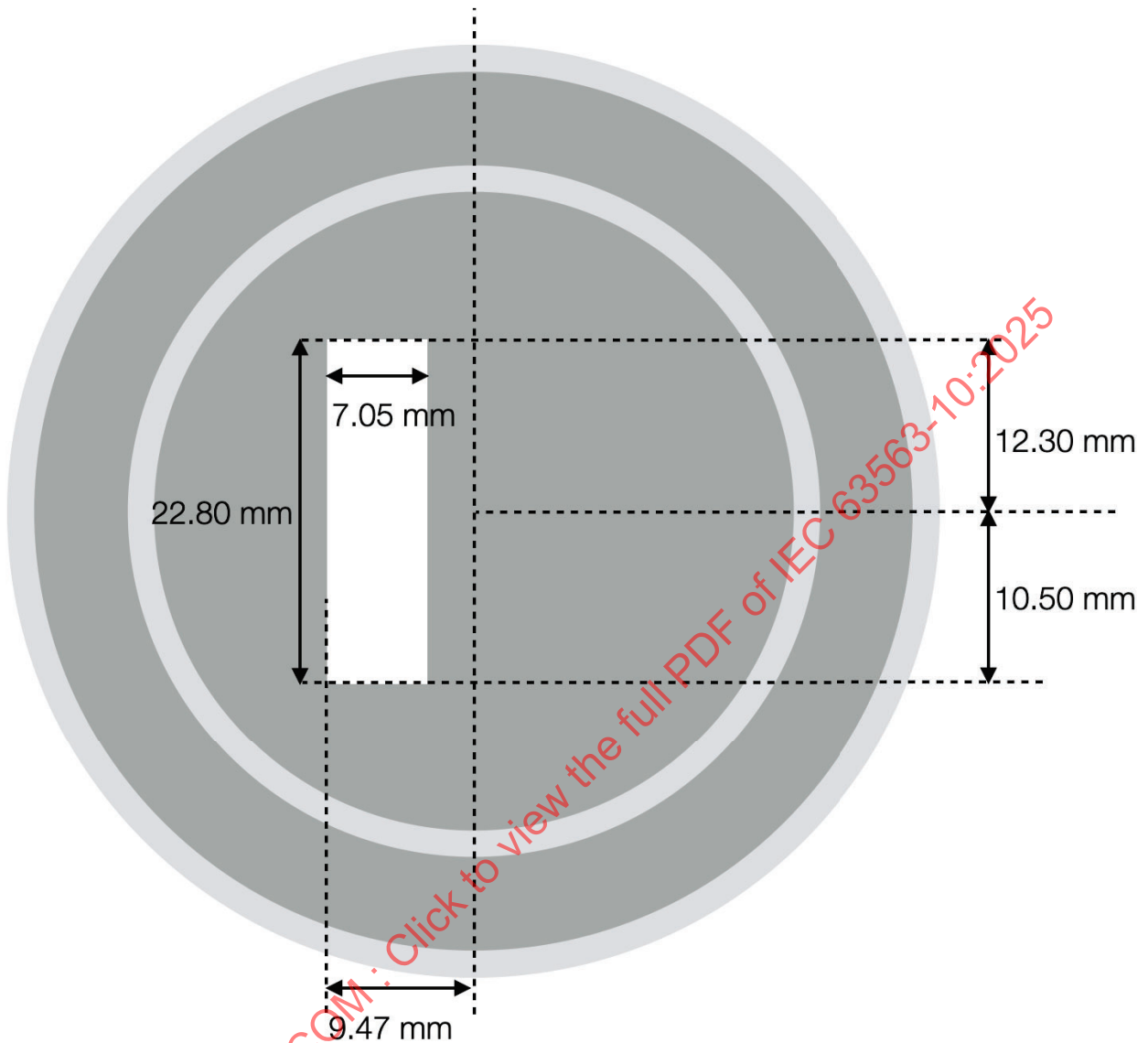


Table 4.2.1.7.3 Mechanical dimensions for the bottom enclosure of the PTx coil system model.

	Description	Nominal Value
d_{enc1}	Bottom enclosure thickness	0.7 mm
d_{enc2}	Enclosure inner wall thickness	0.55 mm
d_{enc3}	Enclosure outer wall thickness	0.7 mm
d_{enc4}	Height of enclosure outer wall	3.25 mm
d_{enc5}	Height of enclosure inner wall	3.04 mm
w_{enc1}	Inner radius of enclosure inner wall	22.12 mm

W_{enc2}	Inner radius of enclosure outer wall	27.48 mm
------------	--------------------------------------	----------

3.2.1.8 Overall Assembly

The assembly of the individual transmitter components described above is outlined below. A side view of the overall assembly of the reference transmitter is shown in Figure 4.2.1.8: 14 . The description and specifications of the key dimensions of the reference transmitter assembly is given in Table 4.2.1.8: 4

Figure 4.2.1.8: 14 Side view of PTx coil system model assembly.

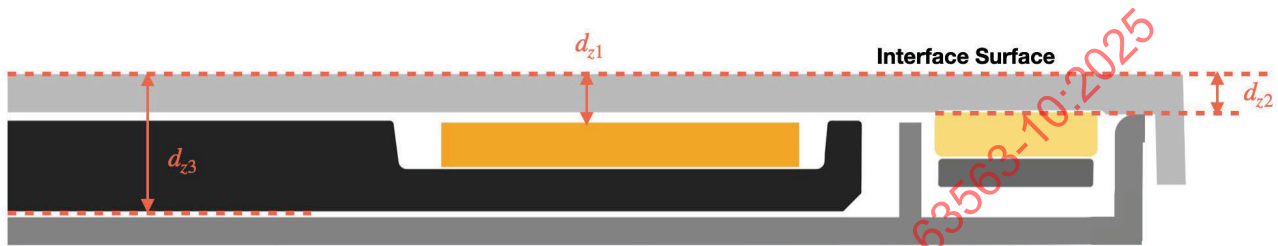


Table 4.2.1.8: 4 Assembly dimensions of PTx coil system model.

	Description	Nominal Value
d_{z1}	Distance from top surface of coil to interface surface	1.20 mm
d_{z2}	Distance from top of magnet surface to interface surface	0.95mm
d_{z3}	Distance from bottom of ferrite to interface surface	3.4mm

3.2.1.9 PTx Orientation Magnets

As discussed in previously sections, the magnet array in the PTx system model follow a ring shape around the coil module and therefore provides radial alignment between the transmitter and receiver coils but allows for rotation around the center of the magnet ring. To ensure the PTx and PRx only aligns in a particular angular direction, an "orientation magnet array" is added to the system model.

3.2.1.9.1 Transmitter-side Orientation Magnet

The top surface of the transmitter orientation magnet is in-plane with the main magnet array discussed in § 4.2.1.4 Coil Module (permanent magnets) . The positioning of the orientation magnets with respect to the main magnet array is shown in Figure 4.2.1.9.1: 15 , wherein the orientation magnet is labeled "clocking magnets". The center of the orientation magnet is aligned with the center of the magnet ring of the PTx coil system. The cross-section of the orientation magnet is shown in Figure 4.2.1.9.1: 16 . The DC shield used in the orientation magnet should use the same material as the DC magnet shunt used in the main magnet array. The B-field strengths in z- and xy-direction are shown in Table 4.2.1.9.1: 5 .

Figure 4.2.1.9.1: 15 Transmitter orientation magnets (Top View).

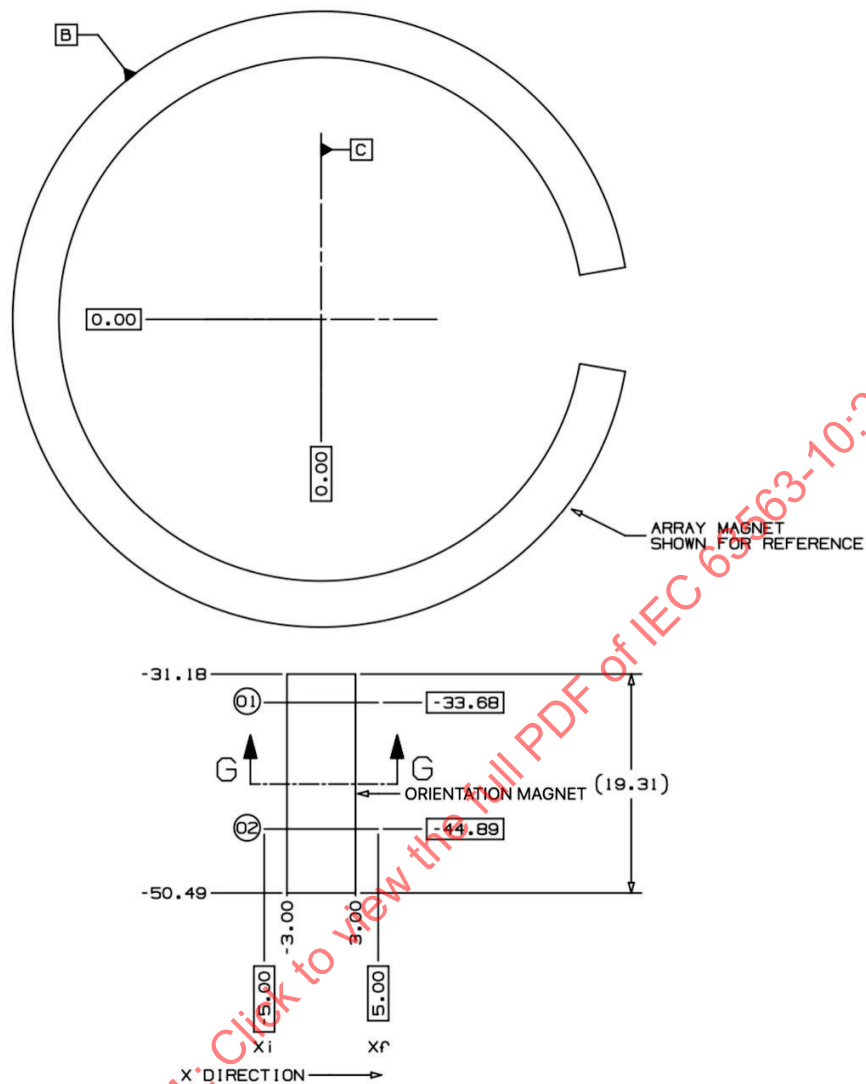


Figure 4.2.1.9.1: 16 Transmitter Orientation Magnet Dimensions and Polarity.

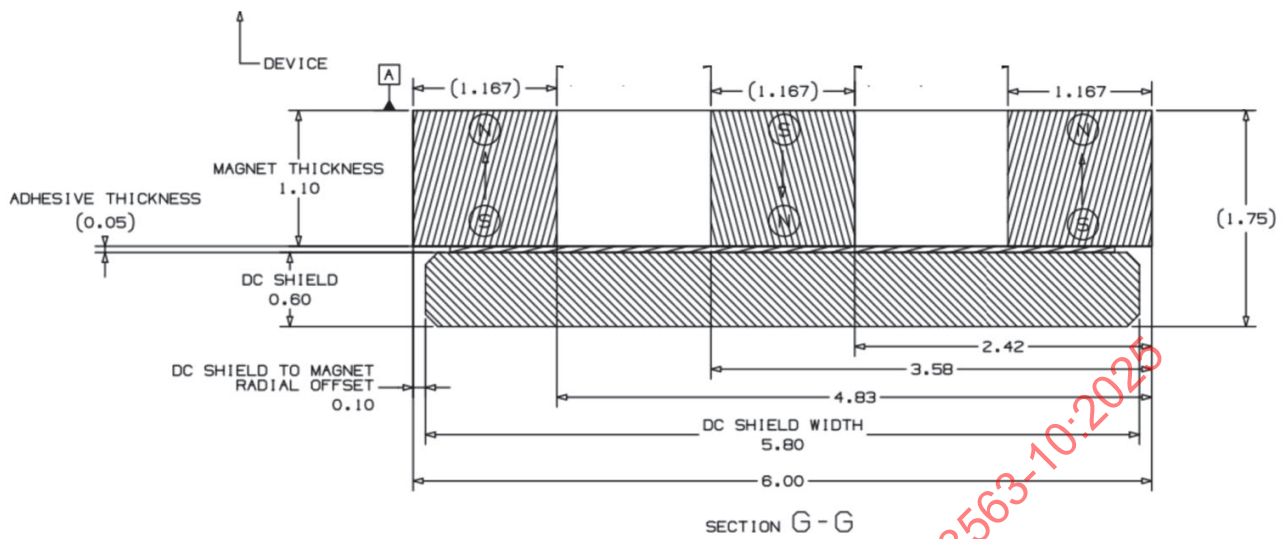


Table 4.2.1.9.1: 5 Flux density at 0.85mm from PTx orientation magnet surface.

Maximum x	Minimum Bz	Bxy
$x < -5.0$ mm	0	0.025
-5.0 mm $< x < 4.5$ mm	0	N/A
-4.5 mm $< x < -3.0$ mm	N/A	0.075 T
-3.0 mm $< x < -2.0$ mm	0.170 T	N/A
-2.0 mm $< x < -0.5$ mm	N/A	0.190 T
-0.5 mm $< x < 0.5$ mm	-0.250 T	N/A
0.5 mm $< x < 2.0$ mm	N/A	0.190 T
2 mm $< x < 3.0$ mm	0.170 T	N/A
3.0 mm $< x < 4.0$ mm	N/A	0.075 T
4.0 mm $< x < 5.0$ mm	0	N/A
$x > 5.0$ mm	0	0.025

* The $z=0$ plane refers to the interface surface, and $x=0/y=0$ refers to the center of the magnetic array.

3.2.2 Electrical Properties

3.2.2.1 Electrical Parameters of PTx coil system model

When the mechanical components are assembled as specified above, the PTx coil system model has the electrical parameters described in Table 4.2.2.1: 6 .

These values are valid under free-air conditions where there is no metallic or magnetic object present in the vicinity of the PTx.

Table 4.2.2.1: 6 Electrical Parameters of the PTx Coil System Model in Free-Air.

	Measurement Frequency	Description	Nominal Value
R _{DC}	N/A	DC resistance between coil terminals of the PTx coil system model	41 mΩ
L _{TX}	360kHz	Self-inductance between coil terminals of the PTx coil system model	7.42 μH
R _{AC}	360kHz	AC resistance between coil terminals of the PTx coil system model	260 mΩ

3.2.2.2 Preventing Saturation of PRx Shielding

The presence of magnets in an MPP PTx induces a DC bias flux in the Shielding of a PRx unit.

For proper operation, the magnetic Shielding must be operated in the non-saturated part of their B-H curve, away from their magnetic saturation inflection point.

Proper power delivery will be impeded if the Shielding of a PRx is allowed to saturate. For typical nano-crystalline (NC) Shielding materials, the saturation flux density is greater than 1T.

The risk of saturation is defined with reference to the TPR#MPP3, which is identical to TPR#MPP1 in all ways except that the number of nanocrystalline layers have been reduced to 3.

This makes TPR#MPP3 more sensitive to strong magnetic fields and a better candidate to evaluate the risk of PRx shielding saturation due to the PTx magnets.

For MPP, there is a risk of saturation if either of the following are true:

$$\Delta L'_{TPR\#MPP3_{(0,0)}} < 0.2$$

$$\Delta L'_{TPR\#MPP3_{(2,2)}} < -0.3$$

Where $\Delta L'_{TPR\#MPP3_{(0,0)}}$ is the normalized change of inductance of TPR#MPP3 when it is placed directly and in the center of the PTx (r=0mm, z=0mm).

$$\Delta L'_{TPR\#MPP3_{(0,0)}} = \frac{L'_{TPR\#MPP3_{(0,0)}} - L_{TPR\#MPP3_{Free Air}}}{L_{TPR\#MPP3_{Free Air}}}$$

And $\Delta L'_{TPR\#MPP3_{(2,2)}}$ is the normalized change of inductance of TPR#MPP3 when it is placed with a radial offset of 2mm from the center of the PTx and a 2mm spacer is present between the TPR and PTx. (r=2mm, z=2mm).

$\Delta L'_{TPR\#MPP3_{(2,2)}}$ is the minimum value when measured in all four directions e.g. (X, Y, Z) = (0,2,2), (0,-2,2), (2,0,2) and (-2,0,2).

$$\Delta L'_{TPR\#MPP3_{(2,2)}} = \frac{L'_{TPR\#MPP3_{(2,2)}} - L_{TPR\#MPP3_{Free Air}}}{L_{TPR\#MPP3_{Free Air}}}$$

The rationale of using $\Delta L'$ to detect saturation is as follows: under normal, unsaturated scenarios, $\Delta L'$ is positive as the ferromagnetic material on PTx helps to increase the inductance of PRx. But if the dc magnet saturates the PRx shielding (e.g., nano-crystalline shielding), then it effectively neutralizes the positive effect on PRx inductance brought by the shielding material and thus $\Delta L'$ will reduce. Additionally, the metallic material in PTx will also reduce $\Delta L'$ through the eddy-current effect. The compound effect will bring $\Delta L'$ down to zero or even negative.

Since (2,2) position has more offset than (0,0), it generally may introduce my saturation, that's why $\Delta L'_{\text{TPR}\#\text{MPP3}(2,2)}$ is smaller than $\Delta L'_{\text{TPR}\#\text{MPP3}(0,0)}$

3.3 PRx Coil System Model

3.3.1 Mechanical Construction

3.3.1.1 Overall Assembly

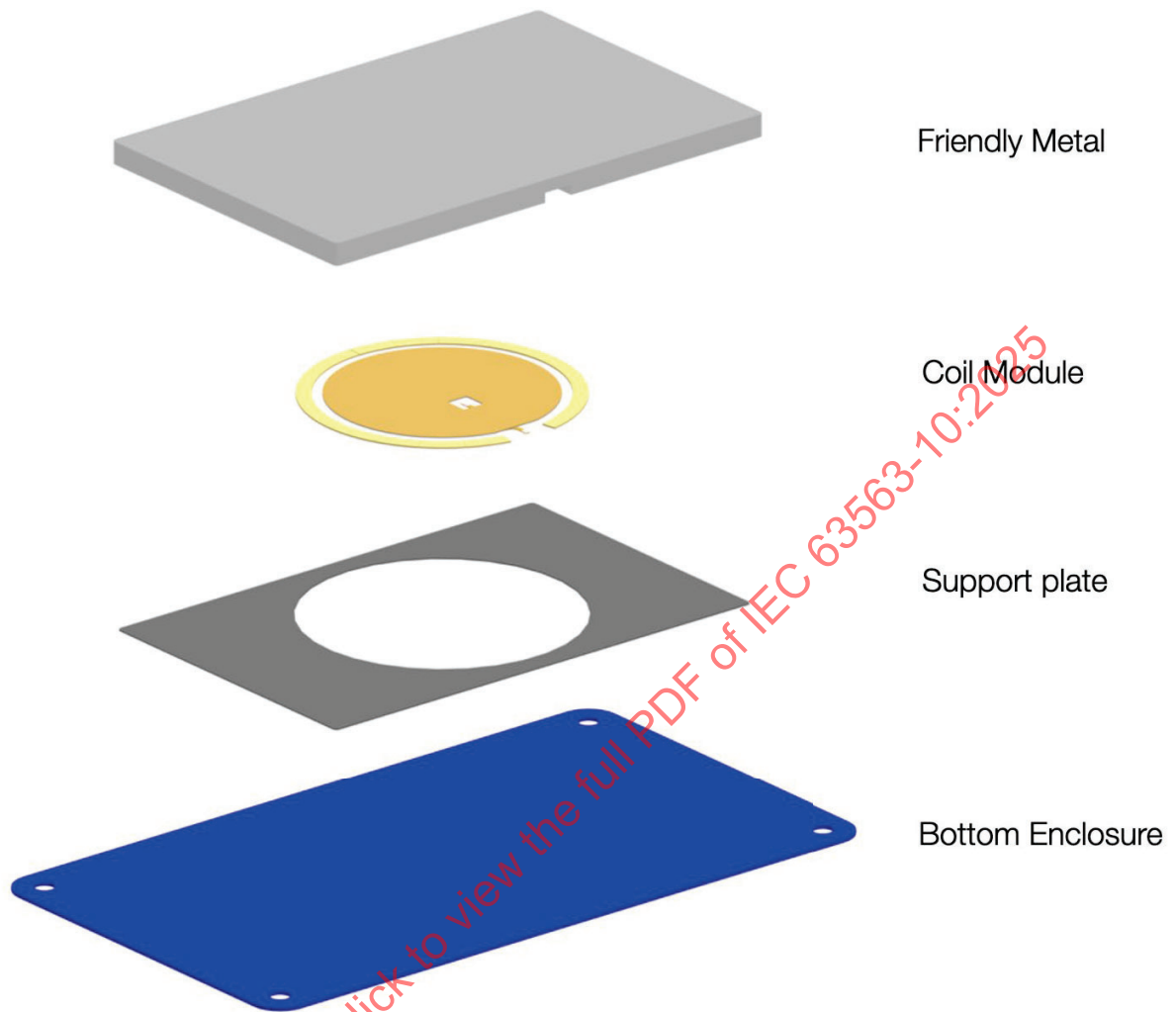
The overall design of the PRx coil system model is shown in Figure 4.3.1.1: 17 . It consists of four main components:

- bottom enclosure that defines the interface surface
- metal support plate
- coil module for wireless power transfer
- metal structure above the coil module defined as a “friendly-metal block”

In Figure 4.3.1.1: 17 the “friendly-metal block” is opaque, to denote that it is not intended to be part of a "real-world" PRx design (but its inclusion in the PRx coil system model is critical in ensuring interoperability). More details regarding the “friendly-metal block” are provided in § 4.3.1.6 Friendly Metal Block .

IECNORM.COM : Click to view the full PDF of IEC 63563-10:2025

Figure 4.3.1.1: 17 Exploded view of PRx coil system model.



3.3.1.2 Bottom Enclosure

The bottom enclosure is constructed using glass.

3.3.1.3 Support Plate

The support plate of the PRx System Model is constructed using 6061 aluminum. The mechanical dimensions of the support plate can be found in Table 4.3.1.7: 11 .

3.3.1.4 Coil Module

The coil module of the PRx coil system model consists of four components:

- copper shielding
- magnetic shielding
- coil
- magnet array

An exploded view of the receiver coil module is shown in Figure 4.3.1.4: 18 .

A cross-sectional view of the coil module is shown in Figure 4.3.1.4: 19 .

The copper shielding aids to decouple the magnetic parameters of the PRx coil module from other system modules that may be present behind the coil module. Additionally, it also aids to minimize coexistence issues between the inductive charging system and other system modules.

The magnetic shielding in the PRx coil system model consists of a base layer and a center post. The base layer is constructed by stacking 7 layers of circular nano-crystalline sheets above the PRx coil. The center post is constructed by stacking 4 layers of nano-crystalline sheets. The specifications for the mechanical dimensions of the Shielding can be found in Table 4.3.1.4: 7 .

Figure 4.3.1.4: 18 Exploded view of the coil module for the PRx coil system model.

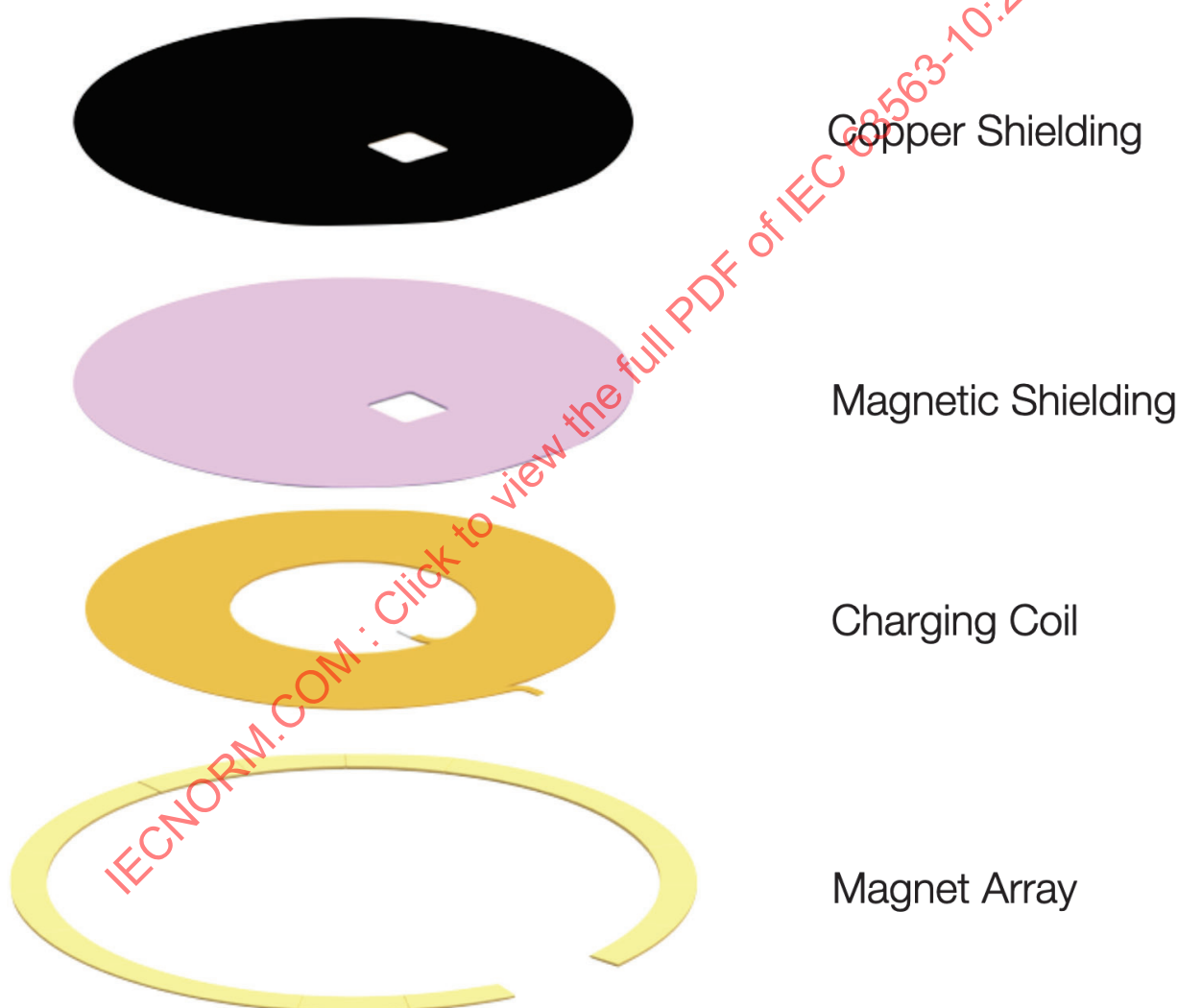


Figure 4.3.1.4: 19 Cross-section of the coil module for the PRx coil system model.



Table 4.3.1.4: 7 Assembly specifications of coil module for the PRx coil system model.

	Description	Nominal Value
w_{Rx1}	Radius of Shielding center post	8.95mm
w_{Rx2}	Radius of Shielding base layer	21.60mm
w_{Rx3}	Radius of Cu shield	21.60mm
d_{Rx1}	Center post shielding material thickness	80µm
d_{Rx2}	Base layer shielding material thickness	179 µm
d_{Rx3}	Cu shielding material thickness	30µm

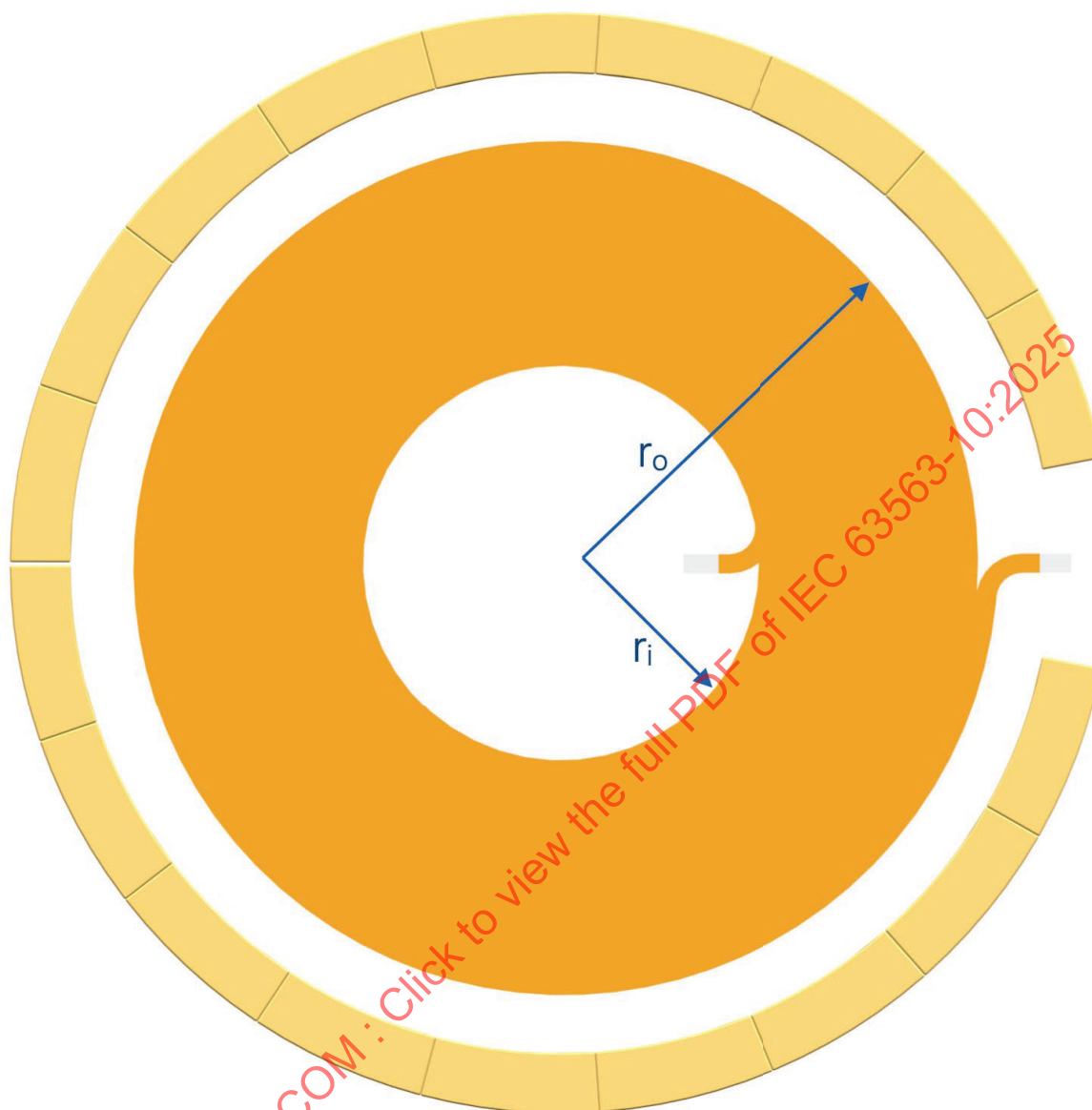
The top and cross-sectional view of the PRx coil system model is shown in Figure 4.3.1.4: 21 and Figure 4.3.1.4: 20, respectively. The receiver coil consists of a 1-layer of copper wires wound in 13 turns. To facilitate access to the coil terminals in practical designs, a cut-out exists in the Shielding to expose the coil leads. As shown in Figure 4.3.1.4: 21, one edge of the cutout is aligned with the geometric center of the Shielding. The mechanical dimensions of the PRx coil can be found in Table 4.3.1.4: 8.

Figure 4.3.1.4: 20 Cross-sectional view of coil for the PRx coil system model.

This diagram shows one turn with multiple strands in parallel. See Table 4.3.1.4: 8.



Figure 4.3.1.4: 21 Top view of PRx coil system model.



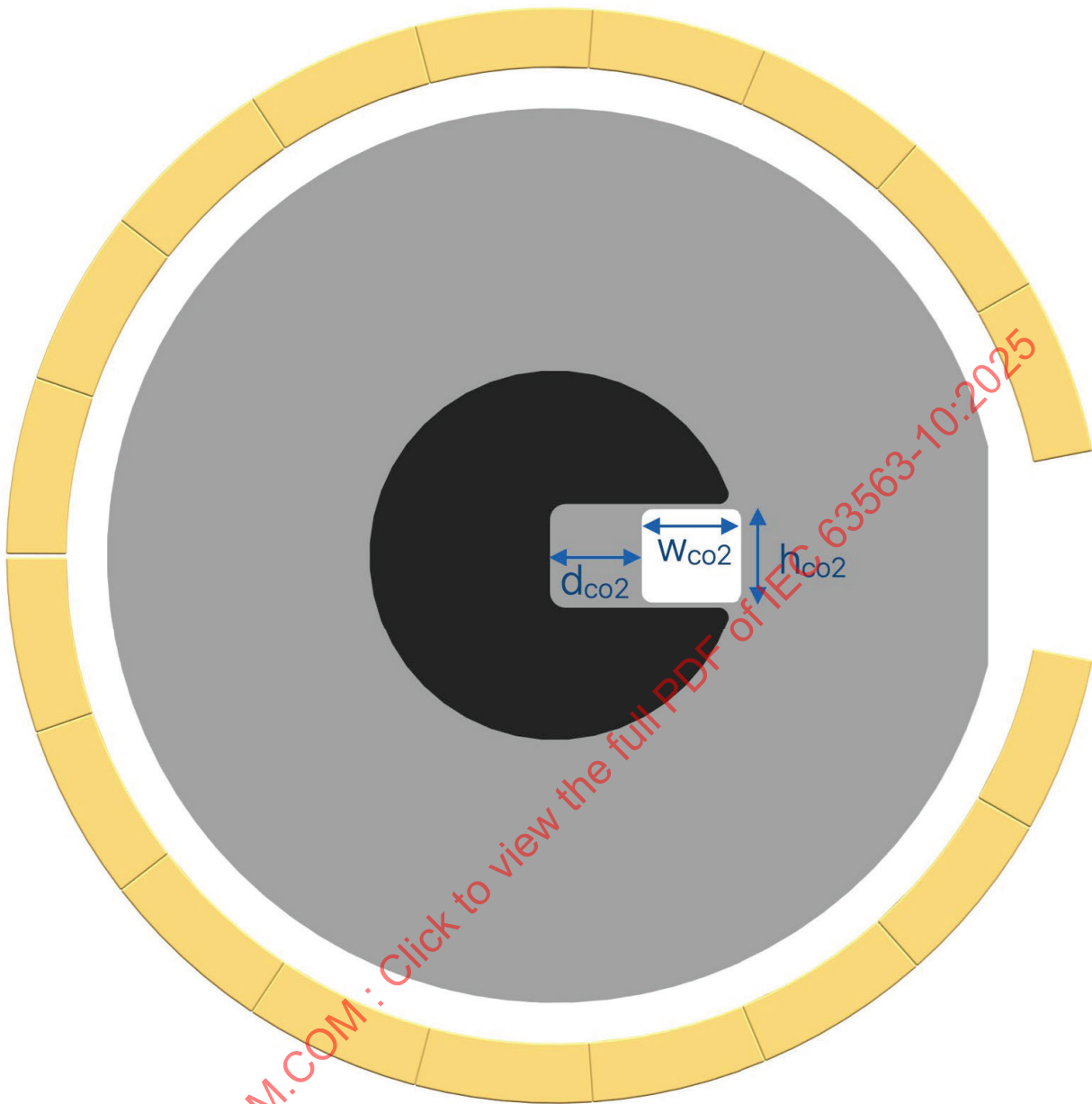


Table 4.3.1.4: 8 Mechanical specifications of the PRx coil system model.

	Description	Nominal Value
r_0	Outer radius of PRx coil	21.00 mm
r_i	Inner radius of PRx coil	9.50 mm
h_{co2}	Height of shielding cutout	4.50 mm
W_{co2}	Width of shielding cutout	4.85 mm
d_{co2}	Offset of shielding cutout from coil center	4.21 mm
W_{cl1}	Diameter of Cu Wire	114 μ m
W_{cl2}	Diameter of wire with insulation	131 μ m

N	Number of turns	13
N _c	Number of strands in parallel per turn (See Figure 4.3.1.4: 20)	7

3.3.1.5 Coil Module (permanent magnets)

Details of the magnet module dimensions are outlined in Figure 4.3.1.5: 22 , and Figure 4.3.1.5: 23 . The magnet module consists of magnet array elements arranged in a circle around the coil module.

The magnetic field values, as measured at the interface surface of the PRx Coil System Model, have been defined in Figure 4.3.1.5: 24 .

In Figure 4.3.1.5: 22 , an additional magnet (labeled "orientation magnet") is also included below the circular magnet array.

The orientation magnet assembly consists of a N48SH magnet and a thin shield above the magnet. The cross-sectional view of the PRx orientation magnet is shown in Figure 4.3.1.5: 25 .

The choice of materials for the construction of the permanent magnet module (including the circular magnet array and the orientation magnet) are outlined in Table 4.3.1.5: 9 .

Table 4.3.1.5: 9 Magnet properties of the PRx coil system model.

Component	Material parameter	Typical values
Magnet array	Br	1.39 T
	H _{cb}	> 1.054 x 10 ⁶ A/m
	H _{cj}	> 1.671 x 10 ⁶ A/m
	BH _{max}	3.7 x 10 ⁵ T•A/m
Permeable shunt	B _{sat}	> 2.0 T

Figure 4.3.1.5: 22 Magnet of the PRx coil system model (top view).

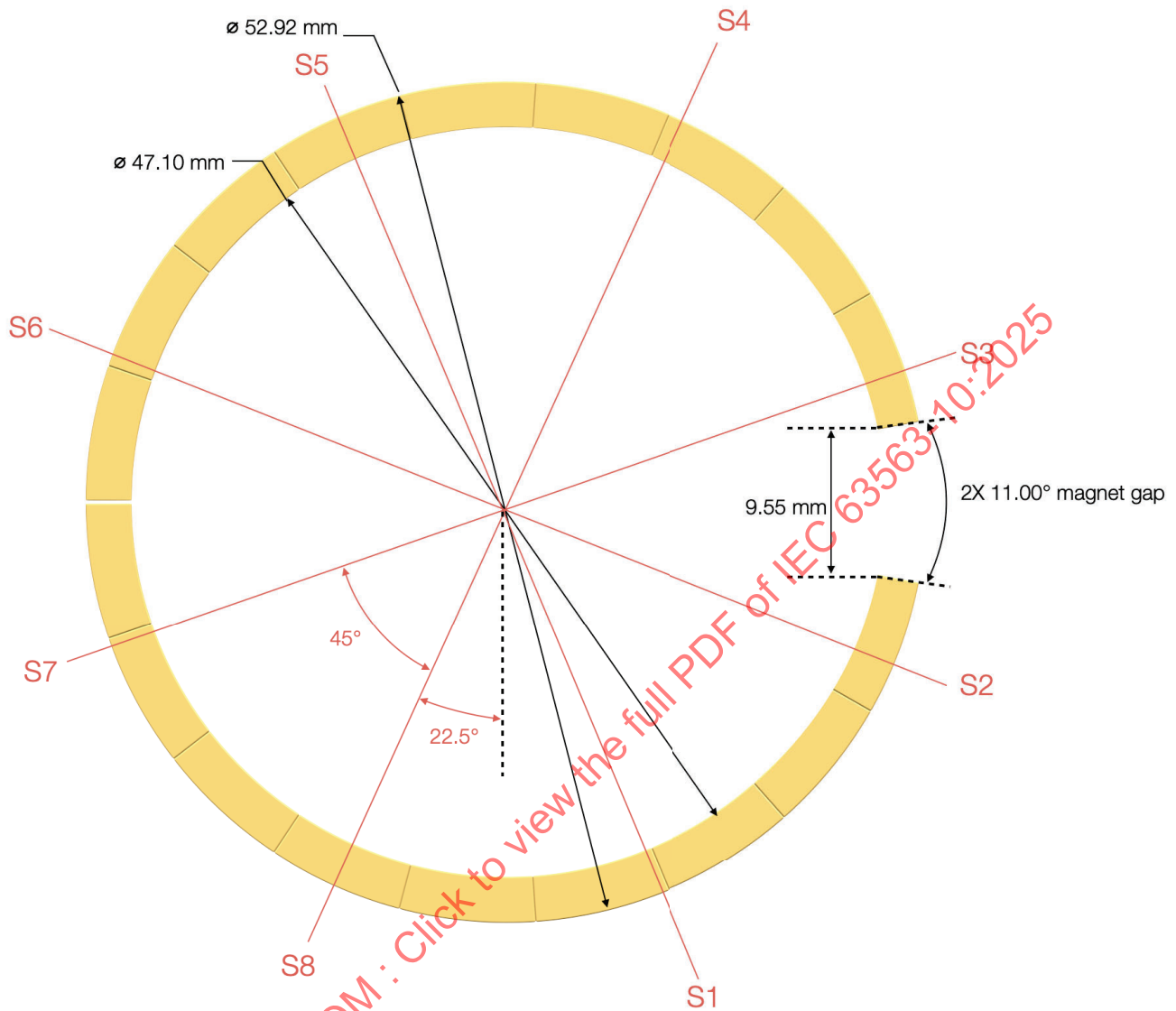


Figure 4.3.1.5: 23 Magnet of the PRx coil system model (side view).

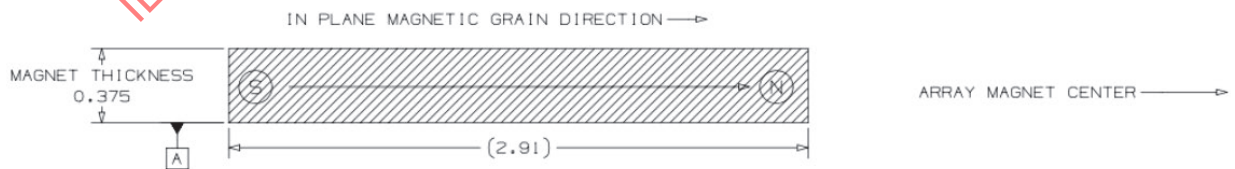
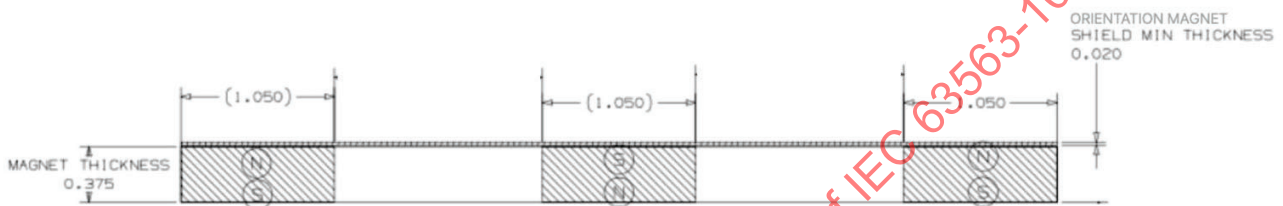


Figure 4.3.1.5: 24 Magnetic field of the PRx coil system model.

Radial Position (mm)	B _z (T)	B _{xy} (T)
$r < 19.5$	0	0.025
$19.5 < r < 23$	N/A	0.050
$23 < r < 24$	-0.0875	N/A
$24.5 < r < 25.5$	N/A	0.0825
$26 < r < 27$	0.0875	N/A
$27 < r < 30$	N/A	0.050
$r > 30$	-0.025	0.025

* The $z=0$ plane refers to the interface surface, and $r=0$ refers to the center of the magnetic array.

Figure 4.3.1.5: 25 Orientation magnet of the PRx coil system model (side view).



3.3.1.6 Friendly Metal Block

In a practical PRx implementation, it is likely that the coil module is surrounded by metallic components (such as battery, PCB), hereafter referred to as “friendly metal”. The friendly metal block shown in Figure 4.3.1.1: 17 is included in the PRx coil system model to represent such metallic components.

In the PRx coil system model, the friendly metal block is made from 316 grade stainless steel. The thickness of the friendly metal block is 4.30mm.

3.3.1.7 Overall Assembly

The assembly of the individual components of the PRx coil system model are outlined below.

A side view of the overall assembly of the PRx coil system model is shown in Figure 4.3.1.7: 26 . Description and dimensions of the assembly can be found in Table 4.3.1.7: 10 .

Figure 4.3.1.7: 26 Cross-sectional view showing assembly of PRx coil system model.



Table 4.3.1.7: 10 Assembly specifications for the PRx coil system model.

	Description	Nominal Value
d_{z1}	Distance from bottom of coil surface to Interface surface	0.660mm
d_{z2}	Distance from bottom of magnet surface to Interface surface	0.660mm
d_{z3}	Distance from bottom of support plate to Interface surface	0.700mm
d_{z4}	Distance from bottom of friendly metal block to Interface surface	1.23mm

Table 4.3.1.7: 11 Mechanical dimensions of support plate.

	Description	Nominal values
t_{SP}	Thickness of support plate	0.2 mm
r_{SP}	Radius of inner cutout of support plate	26.73 mm

3.3.2 Electrical Properties

3.3.2.1 Electrical Parameters of PRx Coil System Model

With the mechanical components assembled as specified above, the PRx coil system model has the electrical parameters described in Table 4.3.2.1: 12 .

These values are valid under free-air conditions. For the electrical parameters of the PTx coil system model when it is mated to the PRx coil system model refer to § 4.4 Properties of Mated Coil System Models .

Table 4.3.2.1: 12 Electrical Parameters of the PRx Coil System Model in Free-Air.

	Measurement Frequency	Description	Nominal Value
R_{DC}	N/A	DC resistance of the receiver measured at the coil terminals	200 mΩ
L_{RX}	360kHz	Self-inductance of the receiver measured at the coil terminals	9.01 μH
R_{AC}	360kHz	AC resistance of the receiver measured at the coil terminals	751 mΩ

3.4 Properties of Mated Coil System Models

3.4.1 Electrical measurement under mated conditions

The electrical parameters for the PTx and PRx coil system models under mated conditions are presented as a guideline for the design of compliant MPP PTx and PRx implementations. To this end, two cases are presented:

- In the first scenario, the PRx coil system model is placed directly on the surface of the PTx coil system model. This case (referred to as “z=0mm” test case), represents the nominal usage case where there is no spacing between the transmitter and the receiver and the two coils are aligned.
- In the second scenario, an air gap of 2mm is introduced between the PRx and PTx coil system models. This case (referred to as “z=2mm” test case), represents the usage scenario where a user may have an accessory attached to the PRx (e.g., a protective case) while charging.
- In both test cases, the PTx and PRx coils should be aligned (radial offset $r = 0\text{mm}$).

The electrical parameters to be measured under mated conditions include: L_{TX}' , L_{RX}' , R_{TX}' , R_{RX}' , K_i and K_r .

The description of these parameters and their expected values for both test cases are given in Table 4.4.1: 13 and Table 4.4.1: 14

Table 4.4.1: 13 Mated electrical parameters (Test case: $r=0$, $z=0$ mm).

	Description	Frequency	Nominal Value
L_{TX}'	Self-inductance at the coil terminals of the PTx coil system model	360kHz	14.80 μH
L_{RX}'	Self-inductance at the coil terminals of the PRx coil system model	360kHz	17.86 μH
R_{TX}'	AC resistance at the coil terminals of the PTx coil system model	360kHz	1.208 Ω
R_{RX}'	AC resistance at the coil terminals of the PRx coil system model	360kHz	1.938 Ω
K_i	Magnetic coupling between the PTx and PRx coil system models	360kHz	0.887
K_r	Resistive coupling between the PTx and PRx coil system models	360kHz	0.870

Table 4.4.1: 14 Mated electrical parameters (Test case: $r=2$, $z=2$ mm).

	Description	Frequency	Nominal Value
L_{TX}'	Self-inductance at the coil terminals of the PTx coil system model	360kHz	10.09 μH
L_{RX}'	Self-inductance at the coil terminals of the PRx coil system model	360kHz	12.09 μH
R_{TX}'	AC resistance at the coil terminals of the PTx coil system model	360kHz	0.630 Ω
R_{RX}'	AC resistance at the coil terminals of the PRx coil system model	360kHz	1.254 Ω

K_i	Magnetic coupling between the PTx and PRx coil system models	360kHz	0.700
K_r	Resistive coupling between the PTx and PRx coil system models	360kHz	0.760

3.5 Coil Specifications

A MPP Magnetic Boundary (MPPMB) is defined to increase the confidence of certified devices interoperability. The overall boundary consists of a set of individual boundaries defined for pairs of highly correlated parameters (L'_{RX} , L'_{TX} , K_i and R'_{RX} , R'_{TX}). Low correlation parameter(s) (K_r) are defined with minimum and maximum limits. Table 1 lists the correlation between parameters set.

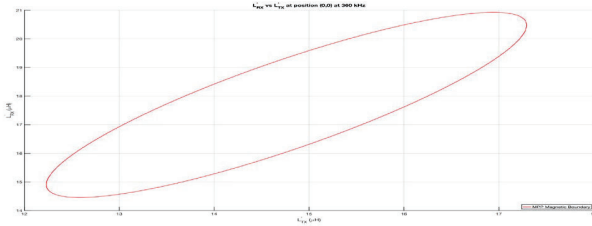
Table 1: Inductive parameter set correlation

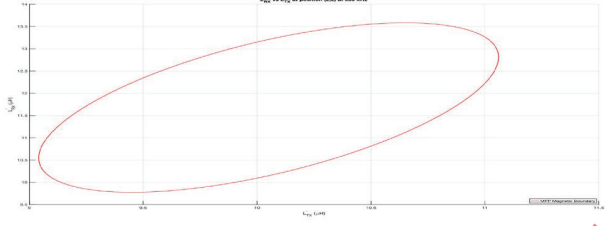
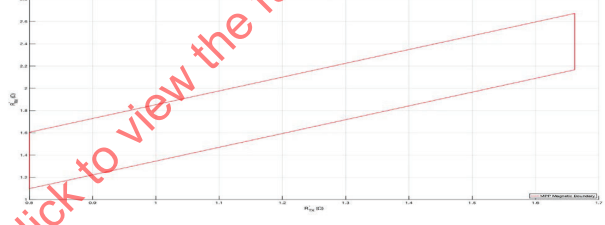
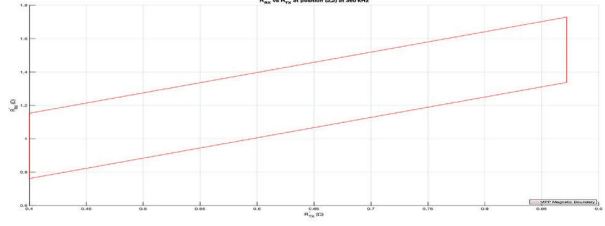
Set	Parameter	Correlation
1	L'_{RX} , L'_{TX} and K_i	High
2	R'_{RX} and R'_{TX}	High
3	K_r	Low

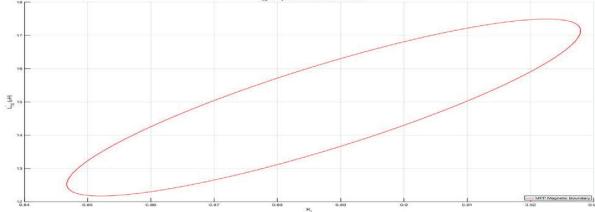
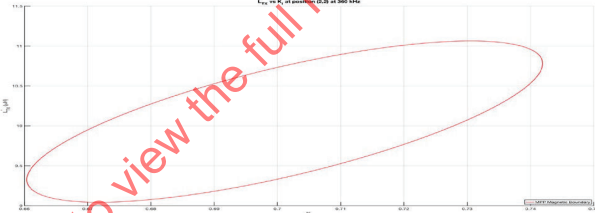
The MPPMB is defined at 128kHz and 360kHz for positions (0,0) and (2,2). The product-to-product mated coil magnetic parameters shall fit within the MPPMB to guarantee feature performance with all certified PTxs and PRxs. A coil design including all process and mechanical tolerances shall meet all the frequency and position boundaries.

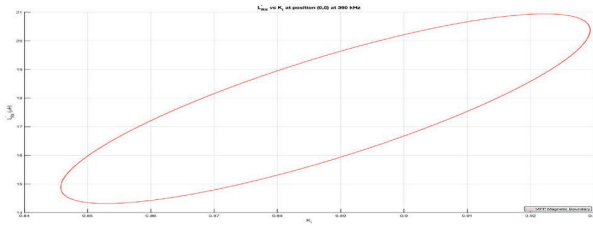
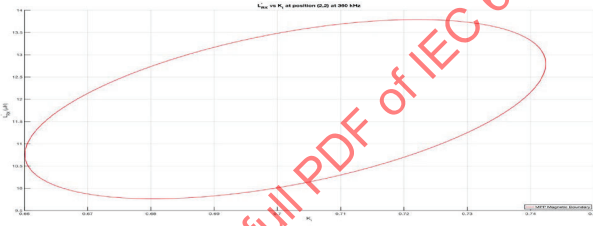
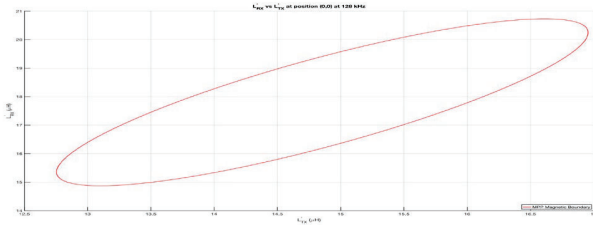
It is recommended that the mated coil parameters should not be close to the edges of the boundary as it risks falling out of the MPPMB when mated to other certified devices.

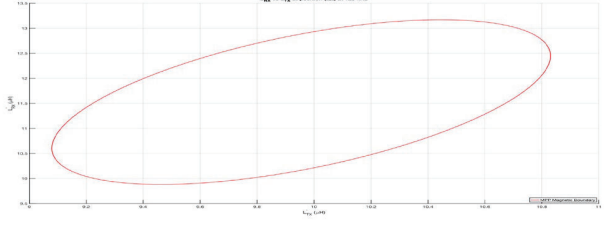
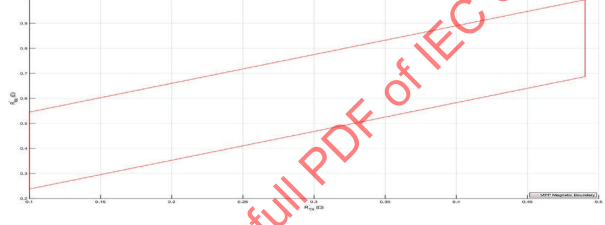
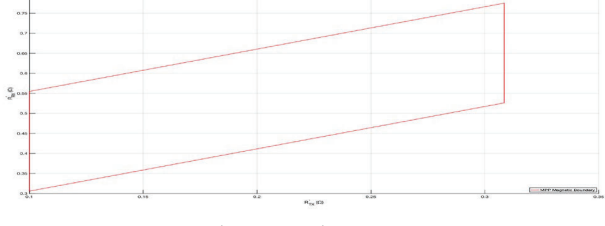
3.5.1 PRx Coil Specifications

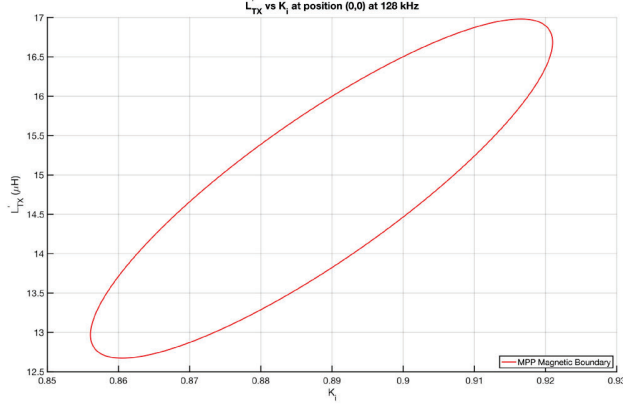
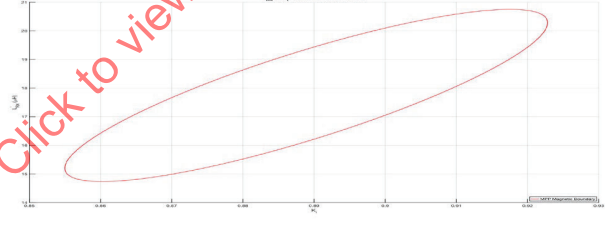
Section	Specification	Description
4.5.1.1	PRx Coil Spec 1	<p>When placing the PRx onto the TPT-Coil, it shall be aligned by the PRx magnets so that the center of the PRx coil is within a 2mm radius of the center of the TPT-Coil.</p> <p>The following TPTs shall be used for this test:</p> <ul style="list-style-type: none"> TPT#MPP1-COIL1 TPT#MPP2-COIL1 TPT#MPP2-COIL2 TPT#MPP2-COIL3
4.5.1.2	PRx Coil Spec 2	<p>The inductance of the PRx coil module when it is mated with PTx at position (0,0) at 360kHz, $L'_{TX(0,0)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to L'_{TX} boundary is described with the equation.</p> $\frac{((L'_{TX} - L'_{TX(prim)}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(prim)}) \sin(\pi - \alpha))^2}{a^2} + \frac{((L'_{TX} - L'_{TX(prim)}) \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(prim)}) \sin(\pi - \alpha))^2}{b^2} = 1$

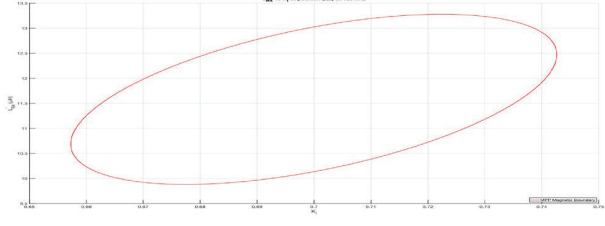
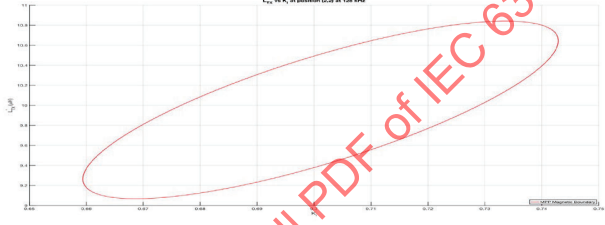
Section	Specification	Description
		<p>where,</p> <p>$(L'_{RX(\text{origin})}, L'_{TX(\text{origin})})$ is the origin of the boundary at (14.7622, 17.6911)</p> <p>a is the length of the long axis, 3.1774</p> <p>b is the length of the short axis, 0.8585</p> <p>α is the rotation from the horizontal axis in radians, 0.6449.</p>
4.5.1.3	PRx Coil Spec 3	<p>The inductance of PRx coil module when it is mated with PTx at position (2,2) at 360kHz, $L'_{TX(2,2)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to L'_{TX} boundary is described with the equation.</p> $\frac{((L'_{TX} - L'_{TX(\text{origin})}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((L'_{TX} - L'_{TX(\text{origin})}) \sin(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \cos(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>$(L'_{RX(\text{origin})}, L'_{TX(\text{origin})})$ is the origin of the boundary at (9.9505, 11.5787)</p> <p>a is the length of the long axis, 1.9938</p> <p>b is the length of the short axis, 0.6790</p> <p>α is the rotation from the horizontal axis in radians, 0.3601.</p>
4.5.1.4	PRx Coil Spec 4	<p>The AC resistance between the coil terminals of the PRx coil module when it is mated with PTx at position (0,0) at 360kHz, $R'_{TX(0,0)}$, shall fit within the boundary defined below.</p>  <p>The relationship between R'_{RX}, and R'_{TX}, can also be described with the equation below:</p> $R'_{RX} = 1.2395 \times R'_{TX} + 0.3597 \Omega \pm 0.2534 \Omega$ <p>for: $0.8000 \Omega \leq R'_{TX} \leq 1.6619 \Omega$</p>
4.5.1.5	PRx Coil Spec 5	<p>The AC resistance between the coil terminals of the PRx coil module when it is mated with PTx at position (2,2) at 360kHz, $R'_{TX(2,2)}$, shall fit within the boundary defined below.</p>  <p>The relationship between R'_{RX}, and R'_{TX}, can also be described with the equation below:</p> $R'_{RX} = 1.2208 \times R'_{TX} + 0.4691 \Omega \pm 0.1956 \Omega$ <p>for: $0.4000 \Omega \leq R'_{TX} \leq 0.8719 \Omega$</p>

Section	Specification	Description
4.5.1.6	PRx Coil Spec 6	<p>The magnetic coupling between the PRx coil module and PTx at position (0,0) at 360kHz, $K_i(0,0)$, given an $L'_{TX}(0,0)$, shall fit within the boundary defined below.</p>  <p>The L'_{TX} to K_i boundary is described with the equation.</p> $\frac{(K_i - K_{i(\text{origin})})^2 \cos^2(\pi - \alpha) + (L'_{TX} - L'_{TX(\text{origin})})^2 \sin^2(\pi - \alpha)}{a^2} + \frac{(K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) - (L'_{TX} - L'_{TX(\text{origin})}) \sin(\pi - \alpha)}{b^2} = 1$ <p>where,</p> <p>$(K_{i(\text{origin})}, L'_{TX(\text{origin})})$ is the origin of the boundary at (0.8873, 14.6523)</p> <p>a is the length of the long axis, 2.0474</p> <p>b is the length of the short axis, 0.0202</p> <p>α is the rotation from the horizontal axis in radians, 0.0132.</p>
4.5.1.7	PRx Coil Spec 7	<p>The magnetic coupling between the PRx coil module and PTx at position (0,0) at 360kHz, $K_i(2,2)$, given an $L'_{TX}(2,2)$, shall fit within the boundary defined below.</p>  <p>The L'_{TX} to K_i boundary is described with the equation.</p> $\frac{(K_i - K_{i(\text{origin})})^2 \cos^2(\pi - \alpha) + (L'_{TX} - L'_{TX(\text{origin})})^2 \sin^2(\pi - \alpha)}{a^2} + \frac{(K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) - (L'_{TX} - L'_{TX(\text{origin})}) \sin(\pi - \alpha)}{b^2} = 1$ <p>where,</p> <p>$(K_{i(\text{origin})}, L'_{TX(\text{origin})})$ is the origin of the boundary at (0.7012, 9.533)</p> <p>a is the length of the long axis, 0.9533</p> <p>b is the length of the short axis, 0.0264</p> <p>α is the rotation from the horizontal axis in radians, 0.0291.</p>
4.5.1.8	PRx Coil Spec 8	The resistive coupling between PRx coil module and PTx at position (0,0), $K_{r(0,0)}$, shall be within 0.80643 and 0.91013 when measured at 360kHz.
4.5.1.9	PRx Coil Spec 9	The resistive coupling between the PRx coil module and PTx at position (2,2), $K_{r(2,2)}$, shall be within 0.68114 and 0.81445 when measured at 360kHz.
4.5.1.10	PRx Coil Spec 10	The magnetic coupling between the PRx coil module and PTx at position (0,0) at 360kHz, $K_i(0,0)$, given an $L'_{RX}(0,0)$, shall fit within the boundary defined below.

Section	Specification	Description
		 <p>The L'_{RX} to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>$(K_{i(\text{origin})}, L'_{RX(\text{origin})})$ is the origin of the boundary at (0.8876, 17.6294)</p> <p>a is the length of the long axis, 2.6099</p> <p>b is the length of the short axis, 0.0197</p> <p>α is the rotation from the horizontal axis in radians, 0.0105.</p>
4.5.1.11	PRx Coil Spec 11	<p>The magnetic coupling between the PRx coil module and PTx at position (2,2) at 360kHz, $K_{i(2,2)}$, given an $L'_{RX(2,2)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>$(K_{i(\text{origin})}, L'_{RX(\text{origin})})$ is the origin of the boundary at (0.7013, 11.6579)</p> <p>a is the length of the long axis, 1.7823</p> <p>b is the length of the short axis, 0.0355</p> <p>α is the rotation from the horizontal axis in radians, 0.0104.</p>
4.5.1.12	PRx Coil Spec 12	<p>The inductance of PRx coil module when it is mated with PTx at position (0,0) at 128kHz, $L'_{TX(0,0)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to L'_{TX} boundary is described with the equation.</p> $\frac{((L'_{TX} - L'_{TX(\text{origin})}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((L'_{TX} - L'_{TX(\text{origin})}) \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>$(L'_{RX(\text{origin})}, L'_{TX(\text{origin})})$ is the origin of the boundary at (14.8551, 17.8023)</p> <p>a is the length of the long axis, 2.7763</p> <p>b is the length of the short axis, 0.7990</p> <p>α is the rotation from the horizontal axis in radians, 0.5926.</p>
4.5.1.13	PRx Coil Spec 13	<p>The inductance of PRx coil module when it is mated with PTx at position (2,2) at 128kHz, $L'_{TX(2,2)}$, shall fit within the boundary defined below.</p>

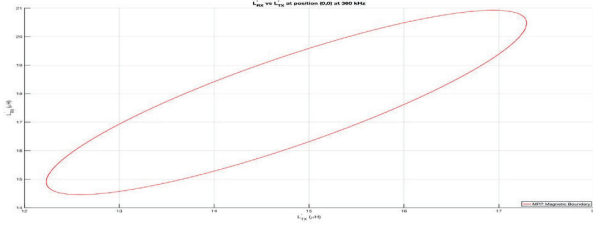
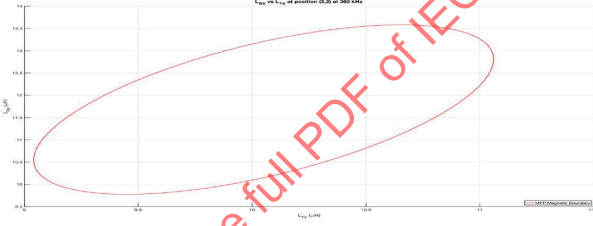
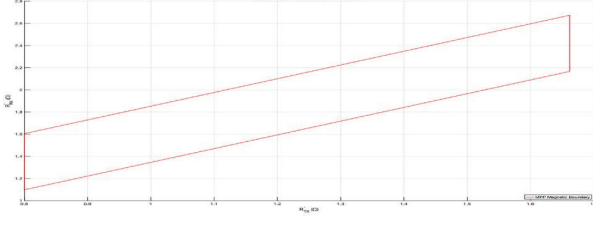
Section	Specification	Description
		 <p>The L'_{RX} to L'_{TX} boundary is described with the equation.</p> $\frac{((L'_{TX} - L'_{TX(\text{origin})}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((L'_{TX} - L'_{TX(\text{origin})}) \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>$(L'_{RX(\text{origin})}, L'_{TX(\text{origin})})$ is the origin of the boundary at (9.9548, 11.5261)</p> <p>a is the length of the long axis, 1.7311</p> <p>b is the length of the short axis, 0.6556</p> <p>α is the rotation from the horizontal axis in radians, 0.3473.</p>
4.5.1.14	PRx Coil Spec 14	<p>The AC resistance between the coil terminals of the PRx coil module when it is mated with PTx at position (0,0) at 128kHz, $R'_{TX(0,0)}$, shall fit within the boundary defined below.</p>  <p>The relationship between R'_{RX} and R'_{TX}, can also be described with the equation below:</p> $R'_{RX} = 1.1500 \times R'_{TX} + 0.2767 \Omega \pm 0.1536 \Omega$ <p>for: $0.1000 \Omega \leq R'_{TX} \leq 0.4903 \Omega$</p>
4.5.1.15	PRx Coil Spec 15	<p>The AC resistance between the coil terminals of the PRx coil module when it is mated with PTx at position (2,2) at 128kHz, $R'_{TX(2,2)}$, shall fit within the boundary defined below.</p>  <p>The relationship between R'_{RX} and R'_{TX}, can also be described with the equation below:</p> $R'_{RX} = 1.0572 \times R'_{TX} + 0.3248 \Omega \pm 0.1245 \Omega$ <p>for: $0.1000 \Omega \leq R'_{TX} \leq 0.3084 \Omega$</p>
4.5.1.16	PRx Coil Spec 16	<p>The magnetic coupling between the PRx coil module and PTx at position (0,0) at 128kHz, $K_{i(0,0)}$, given an $L'_{TX(0,0)}$, shall fit within the boundary defined below.</p>

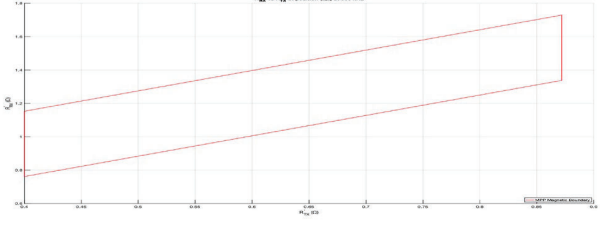
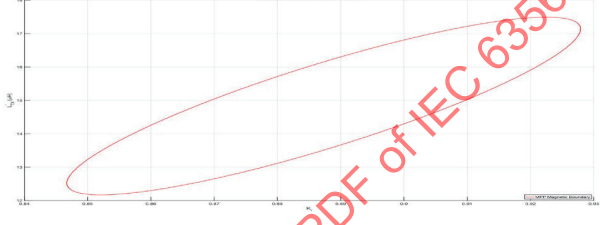
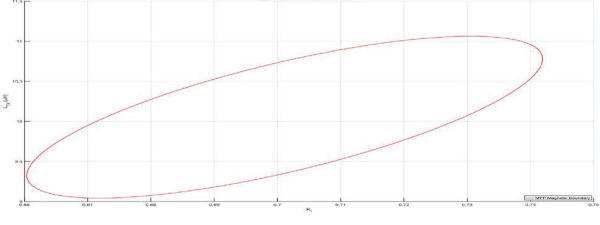
Section	Specification	Description
		 <p>The L'_{TX} to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) + (L'_{TX} - L'_{TX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) - (L'_{TX} - L'_{TX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where, $(K_{i(\text{origin})}, L'_{TX(\text{origin})})$ is the origin of the boundary at (0.8885, 14.8270) a is the length of the long axis, 1.6571 b is the length of the short axis, 0.0164 α is the rotation from the horizontal axis in radians, 0.0130</p>
4.5.1.17	PRx Coil Spec 17	The resistive coupling between PRx coil module and PTx at position (0,0), $K_{i(0,0)}$, shall be within 0.61893 and 0.78638 when measured at 128kHz.
4.5.1.18	PRx Coil Spec 18	The resistive coupling between PRx coil module and PTx at position (2,2), $K_{i(2,2)}$, shall be within 0.53604 and 0.68450 when measured at 128kHz.
4.5.1.19	PRx Coil Spec 19	<p>The magnetic coupling between the PRx coil module and PTx at position (0,0) at 128kHz, $K_{i(0,0)}$, given an $L'_{RX(0,0)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where, $(K_{i(\text{origin})}, L'_{RX(\text{origin})})$ is the origin of the boundary at (0.8889, 17.7432) a is the length of the long axis, 2.3698 b is the length of the short axis, 0.0153 α is the rotation from the horizontal axis in radians, 0.0095</p>
4.5.1.20	PRx Coil Spec 20	The magnetic coupling between the PRx coil module and PTx at position (2,2) at 128kHz, $K_{i(2,2)}$, given an $L'_{RX(2,2)}$, shall fit within the boundary defined below.

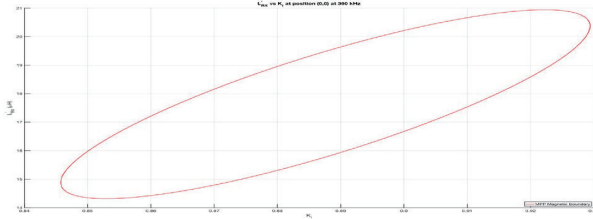
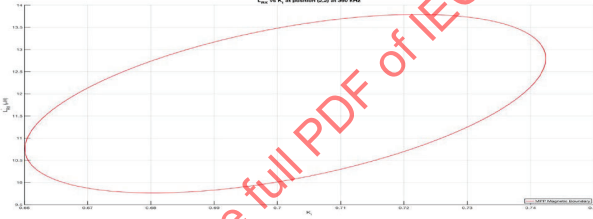
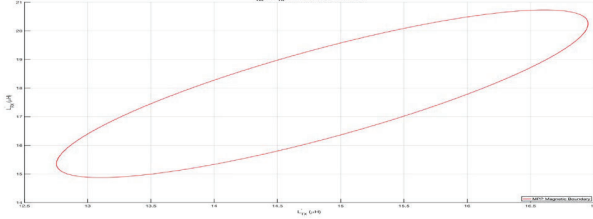
Section	Specification	Description
		 <p>The L'_{RX} to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>$(K_{i(\text{origin})}, L'_{RX(\text{origin})})$ is the origin of the boundary at (0.6999, 11.5812)</p> <p>a is the length of the long axis, 1.6185</p> <p>b is the length of the short axis, 0.0363</p> <p>α is the rotation from the horizontal axis in radians, 0.0132</p>
4.5.1.21	PRx Coil Spec 21	<p>The magnetic coupling between the PRx coil module and PTx at position (2,2) at 128kHz, $K_{i(2,2)}$, given an $L'_{TX(2,2)}$, shall fit within the boundary defined below.</p>  <p>The L'_{TX} to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) + (L'_{TX} - L'_{TX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) - (L'_{TX} - L'_{TX(\text{origin})}) \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>$(K_{i(\text{origin})}, L'_{TX(\text{origin})})$ is the origin of the boundary at (0.7011, 9.9551)</p> <p>a is the length of the long axis, 0.8069</p> <p>b is the length of the short axis, 0.0254</p> <p>α is the rotation from the horizontal axis in radians, 0.0336</p>

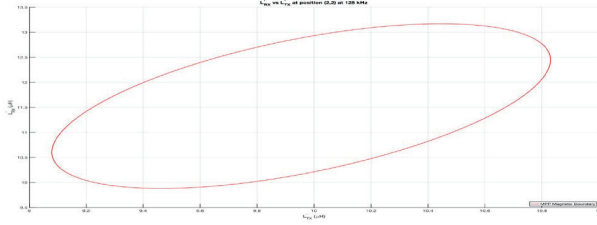
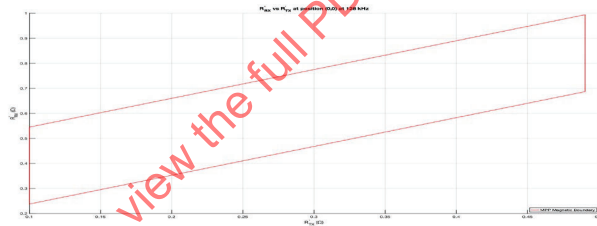
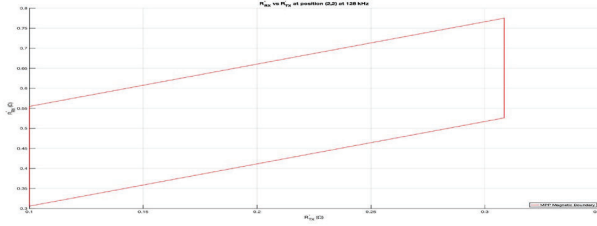
3.5.2 PTx Coil Specifications

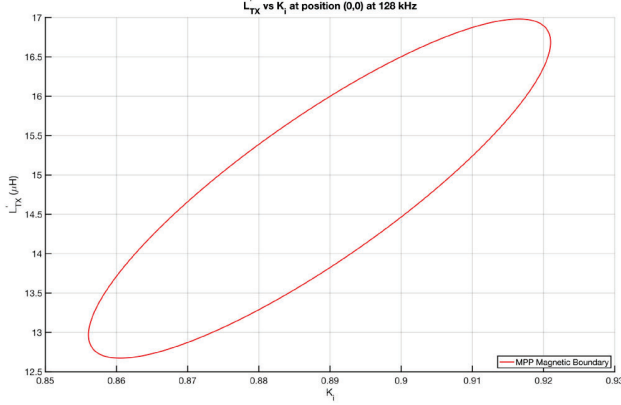

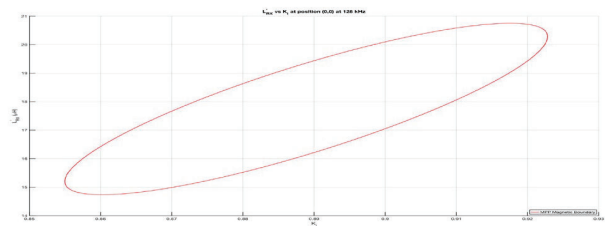
Section	Specification	Description
4.5.2.1	PTx Coil Spec 1	<p>When placing the TPR-Coil onto the PTx, it shall be aligned by the PTx magnets so that the center of the TPR coil is within a 2mm radius of the center of the PTx coil.</p> <p>The following TPRs shall be used for this test:</p> <ul style="list-style-type: none"> TPR#MPP1-COIL1 TPR#MPP2-COIL1 TPR#MPP2-COIL2 TPR#MPP2-COIL3
4.5.2.2	PTx Coil Spec 2	<p>The PTx shall ensure that the magnetic shielding of the TPR#MPP3 is not saturated by the PTx magnets.</p> <p>Note: For this to be true, the following conditions need to be met when the TPR is placed on the PTx:</p> $\Delta L'_{TPR\#MPP3(0,0)} \geq 0.2$ $\Delta L'_{TPR\#MPP3(2,2)} \geq -0.3$

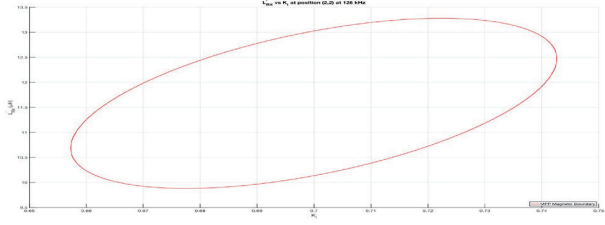
Section	Specification	Description
4.5.2.3	PTx Coil Spec 3	<p>The inductance of PTx coil module when it is mated with the PRx at position (0,0) at 360kHz, $L'_{TX(0,0)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to L'_{TX} boundary is described with the equation.</p> $\frac{((L'_{TX} - L'_{TX(\text{origin})}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((L'_{TX} - L'_{TX(\text{origin})}) \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>($L'_{RX(\text{origin})}$, $L'_{TX(\text{origin})}$) is the origin of the boundary at (14.7622, 17.6911)</p> <p>a is the length of the long axis, 3.1774</p> <p>b is the length of the short axis, 0.8585</p> <p>α is the rotation from the horizontal axis in radians, 0.6449.</p>
4.5.2.4	PTx Coil Spec 4	<p>The inductance of PTx coil module when it is mated with the PRx at position (2,2) at 360kHz, $L'_{TX(2,2)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to L'_{TX} boundary is described with the equation.</p> $\frac{((L'_{TX} - L'_{TX(\text{origin})}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((L'_{TX} - L'_{TX(\text{origin})}) \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>($L'_{RX(\text{origin})}$, $L'_{TX(\text{origin})}$) is the origin of the boundary at (9.9505, 11.5787)</p> <p>a is the length of the long axis, 1.9938</p> <p>b is the length of the short axis, 0.6790</p> <p>α is the rotation from the horizontal axis in radians, 0.3601.</p>
4.5.2.5	PTx Coil Spec 5	<p>The AC resistance between the coil terminals of the PTx coil module when it is mated with the PRx at position (0,0) at 360kHz, $R'_{TX(0,0)}$, shall fit within the boundary defined below.</p>  <p>The relationship between R'_{RX}, and R'_{TX}, can also be described with the equation below:</p> $R'_{RX} = 1.2395 \times R'_{TX} + 0.3597 \Omega \pm 0.2534 \Omega$ <p>for: $0.8000 \Omega \leq R'_{TX} \leq 1.6619 \Omega$</p>
4.5.2.6	PTx Coil Spec 6	<p>The AC resistance between the coil terminals of the PTx coil module when it is mated with the PRx at position (2,2) at 360kHz, $R'_{TX(2,2)}$, shall fit within the boundary defined below.</p>

Section	Specification	Description
		 <p>The relationship between R'_{RX}, and R'_{TX}, can also be described with the equation below:</p> $R'_{RX} = 1.2208 \times R'_{TX} + 0.4691 \Omega \pm 0.1956 \Omega$ <p>for: $0.4000 \Omega \leq R'_{TX} \leq 0.8719 \Omega$</p>
4.5.2.7	PTx Coil Spec 7	<p>The magnetic coupling between the PTx and the PRx at position (0,0) at 360kHz, $K_i(0,0)$, given an $L'_{TX}(0,0)$, shall fit within the boundary defined below.</p>  <p>The L'_{TX} to K_i boundary is described with the equation.</p> $\frac{(K_i - K_{i(prigin)}) \cos(\pi - \alpha) + (L'_{TX} - L'_{TX(prigin)}) \sin(\pi - \alpha)}{a^2} + \frac{(K_i - K_{i(prigin)}) \cos(\pi - \alpha) - (L'_{TX} - L'_{TX(prigin)}) \sin(\pi - \alpha)}{b^2} = 1$ <p>where,</p> <p>$(K_{i(prigin)}, L'_{TX(prigin)})$ is the origin of the boundary at (0.8873, 14.6523)</p> <p>a is the length of the long axis, 2.0474</p> <p>b is the length of the short axis, 0.0202</p> <p>α is the rotation from the horizontal axis in radians, 0.0132.</p>
4.5.2.8	PTx Coil Spec 8	<p>The magnetic coupling between the PTx and the PRx at position (0,0) at 360kHz, $K_i(2,2)$, given an $L'_{TX}(2,2)$, shall fit within the boundary defined below.</p>  <p>The L'_{TX} to K_i boundary is described with the equation.</p> $\frac{(K_i - K_{i(prigin)}) \cos(\pi - \alpha) + (L'_{TX} - L'_{TX(prigin)}) \sin(\pi - \alpha)}{a^2} + \frac{(K_i - K_{i(prigin)}) \cos(\pi - \alpha) - (L'_{TX} - L'_{TX(prigin)}) \sin(\pi - \alpha)}{b^2} = 1$ <p>where,</p> <p>$(K_{i(prigin)}, L'_{TX(prigin)})$ is the origin of the boundary at (0.7012, 9.9533)</p> <p>a is the length of the long axis, 0.9533</p> <p>b is the length of the short axis, 0.0264</p> <p>α is the rotation from the horizontal axis in radians, 0.0291.</p>

Section	Specification	Description
4.5.2.9	PTx Coil Spec 9	<p>The magnetic coupling between the PTx and the PRx at position (0,0) at 360kHz, $K_{i(0,0)}$, given an $L'_{RX(0,0)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>$(K_{i(\text{origin})}, L'_{RX(\text{origin})})$ is the origin of the boundary at (0.0876, 17.6294)</p> <p>a is the length of the long axis, 2.6099</p> <p>b is the length of the short axis, 0.0197</p> <p>α is the rotation from the horizontal axis in radians, 0.0105</p>
4.5.2.10	PTx Coil Spec 10	<p>The magnetic coupling between the PTx and the PRx at position (2,2) at 360kHz, $K_{i(2,2)}$, given an $L'_{RX(2,2)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>$(K_{i(\text{origin})}, L'_{RX(\text{origin})})$ is the origin of the boundary at (0.7013, 11.6579)</p> <p>a is the length of the long axis, 1.7823</p> <p>b is the length of the short axis, 0.0355</p> <p>α is the rotation from the horizontal axis in radians, 0.0104.</p>
4.5.2.11	PTx Coil Spec 11	The resistive coupling between PTx and the PRx at position (0,0), $K_{r(0,0)}$, shall be within 0.80643 and 0.91013 when measured at 360kHz.
4.5.2.12	PTx Coil Spec 12	The resistive coupling between PTx and the PRx at position (2,2), $K_{r(2,2)}$, shall be within 0.68114 and 0.81445 when measured at 360kHz.
4.5.2.13	PTx Coil Spec 13	<p>The inductance of PTx coil module when it is mated with the PRx at position (0,0) at 128kHz, $L'_{TX(0,0)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to L'_{TX} boundary is described with the equation.</p> $\frac{((L'_{TX} - L'_{TX(\text{origin})}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{a^2} + \frac{((L'_{TX} - L'_{TX(\text{origin})}) \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>$(L'_{RX(\text{origin})}, L'_{TX(\text{origin})})$ is the origin of the boundary at (14.8551, 17.8023)</p>

Section	Specification	Description
		<p>a is the length of the long axis, 2.7763</p> <p>b is the length of the short axis, 0.7990</p> <p>α is the rotation from the horizontal axis in radians, 0.5926.</p>
4.5.2.14	PTx Coil Spec 14	<p>The inductance of PTx coil module when it is mated with the PRx at position (2,2) at 128kHz, $L'_{TX(2,2)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to L'_{TX} boundary is described with the equation.</p> $\frac{((L'_{TX} - L'_{TX(origin)}) \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(origin)}) \sin(\pi - \alpha))^2}{a^2} + \frac{((L'_{TX} - L'_{TX(origin)}) \sin(\pi - \alpha) - (L'_{RX} - L'_{RX(origin)}) \cos(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>($L'_{RX(origin)}$, $L'_{TX(origin)}$) is the origin of the boundary at (9.9548, 11.5261)</p> <p>a is the length of the long axis, 1.7311</p> <p>b is the length of the short axis, 0.6556</p> <p>α is the rotation from the horizontal axis in radians, 0.3473.</p>
4.5.2.15	PTx Coil Spec 15	<p>The AC resistance between the coil terminals of the PTx coil module when it is mated with the PRx at position (0,0) at 128kHz, $R'_{TX(0,0)}$, shall fit within the boundary defined below.</p>  <p>The relationship between R'_{RX}, and R'_{TX}, can also be described with the equation below:</p> $R'_{RX} = 1.1500 \times R'_{TX} + 0.2767 \Omega \pm 0.1536 \Omega$ <p>for: $0.1000 \Omega \leq R'_{TX} \leq 0.4903 \Omega$</p>
4.5.2.16	PTx Coil Spec 16	<p>The AC resistance between the coil terminals of the PTx coil module when it is mated with the PRx at position (2,2) at 128kHz, $R'_{TX(2,2)}$, shall fit within the boundary defined below.</p>  <p>The relationship between R'_{RX}, and R'_{TX}, can also be described with the equation below:</p> $R'_{RX} = 1.0572 \times R'_{TX} + 0.3248 \Omega \pm 0.1245 \Omega$ <p>for: $0.1000 \Omega \leq R'_{TX} \leq 0.3084 \Omega$</p>
4.5.2.17	PTx Coil Spec 17	<p>The magnetic coupling between the PTx and the PRx at position (0,0) at 128kHz, $K_{i(0,0)}$, given an $L'_{TX(0,0)}$, shall fit within the boundary defined below.</p>

Section	Specification	Description
		<p>L_{TX}' vs K_i at position (0,0) at 128 kHz</p>  <p>The L_{TX}' to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) + (L'_{TX} - L'_{TX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) - (L'_{TX} - L'_{TX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>(K_{i(origin)}, L_{TX'(origin)}) is the origin of the boundary at (0.8885, 14.8270)</p> <p>a is the length of the long axis, 1.6571</p> <p>b is the length of the short axis, 0.0164</p> <p>α is the rotation from the horizontal axis in radians, 0.0130</p>
4.5.2.18	PTx Coil Spec 18	<p>The magnetic coupling between the PTx and the PRx at position (2,2) at 128kHz, K_{i(2,2)}, given an L_{TX(2,2)}, shall fit within the boundary defined below.</p>  <p>The L_{TX}' to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) + (L'_{TX} - L'_{TX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) - (L'_{TX} - L'_{TX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>(K_{i(origin)}, L_{TX'(origin)}) is the origin of the boundary at (0.7011, 9.9551)</p> <p>a is the length of the long axis, 0.8069</p> <p>b is the length of the short axis, 0.0254</p> <p>α is the rotation from the horizontal axis in radians, 0.0336</p>
4.5.2.19	PTx Coil Spec 19	<p>The magnetic coupling between the PTx and the PRx at position (0,0) at 128kHz, K_{i(0,0)}, given an L_{RX(0,0)}, shall fit within the boundary defined below.</p>  <p>The L_{RX}' to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>(K_{i(origin)}, L_{RX'(origin)}) is the origin of the boundary at (0.8889, 17.7432)</p>

Section	Specification	Description
		<p>a is the length of the long axis, 2.3698</p> <p>b is the length of the short axis, 0.0153</p> <p>α is the rotation from the horizontal axis in radians, 0.0095</p>
4.5.2.20	PTx Coil Spec 20	<p>The magnetic coupling between the PTx and the PRx at position (2,2) at 128kHz, $K_{i(2,2)}$, given an $L'_{RX(2,2)}$, shall fit within the boundary defined below.</p>  <p>The L'_{RX} to K_i boundary is described with the equation.</p> $\frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) + (L'_{RX} - L'_{RX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{a^2} + \frac{((K_i - K_{i(\text{origin})}) \cdot \cos(\pi - \alpha) - (L'_{RX} - L'_{RX(\text{origin})}) \cdot \sin(\pi - \alpha))^2}{b^2} = 1$ <p>where,</p> <p>$(K_{i(\text{origin})}, L'_{RX(\text{origin})})$ is the origin of the boundary at (0.6999, 1.5812)</p> <p>a is the length of the long axis, 1.6185</p> <p>b is the length of the short axis, 0.0363</p> <p>α is the rotation from the horizontal axis in radians, 0.0132</p>
4.5.2.21	PTx Coil Spec 21	The resistive coupling between PTx and the PRx at position (0,0), $K_{r(0,0)}$, shall be within 0.61893 and 0.78638 when measured at 128kHz.
4.5.2.22	PTx Coil Spec 22	The resistive coupling between PTx and the PRx at position (2,2), $K_{r(2,2)}$, shall be within 0.53604 and 0.68450 when measured at 128kHz.

4 Power Delivery

Unless otherwise stated, all contents in the chapter applies to power delivery in MPP mode instead of BPP mode.

4.1 Power Profiles (BPP + MPP)

4.1.1 Specifications

Section	Specification	Description
5.1.1.1	Power Delivery Spec 1	Th PTx shall provide a BPP PRx with at least 5W of rectified power for $0\text{mm} \leq z \leq 3\text{mm}$, $0\text{mm} \leq r \leq 8\text{mm}$ (Figure 4.3.2.1: 28). Note: See § 5.1.3.1 for the definition of z and r.
5.1.1.2	Power Delivery Spec 2	The PTx shall provide a MPP PRx with at least 15W of rectified power inside the 2x2 cylinder ($0\text{mm} \leq z \leq 2\text{mm}$, $0\text{mm} \leq r \leq 2\text{mm}$) Figure 4.3.2.1: 27 .
5.1.1.3	Power Delivery Spec 3	The PTx shall provide a MPP PRx with at least 5W of rectified power for $0 \leq z \leq 3\text{mm}$, $0\text{mm} \leq r \leq 4\text{mm}$.

4.1.2 Recommendations

Section	Specification	Description
5.1.2.1	Power Capability Reduction Spec 1	In MPP mode; For $z > 3\text{mm}$ & $r > 4\text{mm}$, load power delivery should gradually decrease from 5W as distance from the center increases.

4.1.3 Specification Notes

Section	Specification	Description
5.1.3.1	Definition of z and r	MPP devices are required to provide guaranteed performance with respect to externally observable features of the design such as distance between the contact surface of PTx to the contact surface of the PRx. Thus, in the specified power delivery volume below and throughout the MPP specification, when "z" distance is specified it indicates surface-to-surface separation rather than, for instance, the coil-to-coil separation. For example, Figure 4.3.2.1: 29 shows how z gap between a PTx and PRx is defined in the system model. In this example, the PTx and PRx have the same mechanical stack-up as the § 4.2 PTx Coil System Model and § 4.3 PRx Coil System Model . The origin $r=0$ is defined as the location corresponding to maximum coupling when $z=0$.

Figure 4.3.2.1: 27 MPP minimum power delivery requirement shall be $P_I \geq 15\text{W}$ for $0\text{mm} \leq z \leq 2\text{mm}$, $0\text{mm} \leq r \leq 2\text{mm}$.

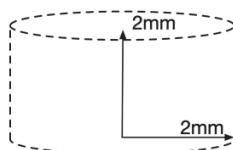


Figure 4.3.2.1: 28 An MPP PTx shall be able to deliver $PI \geq 5W$ to an BPP system model PRx for $0mm \leq z \leq 3mm$,
 $0mm \leq r \leq 8mm$.

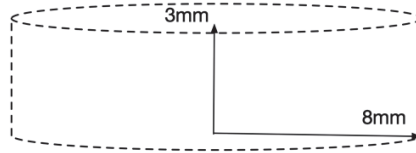
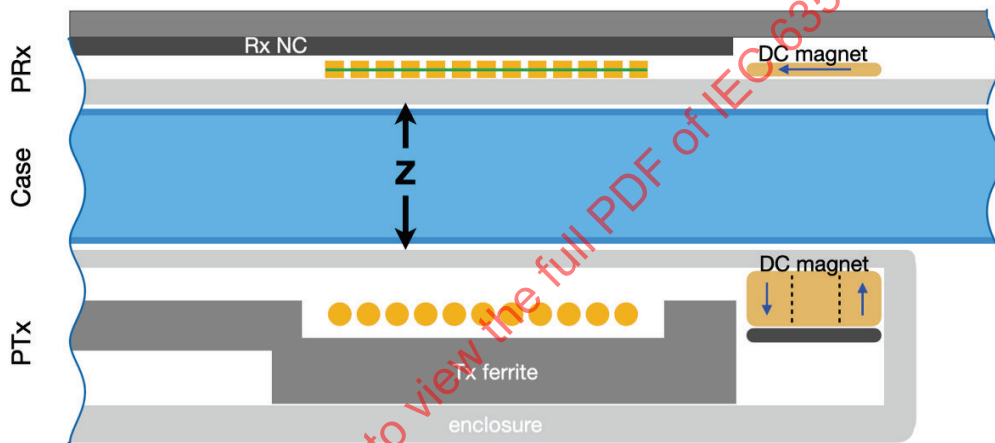


Figure 4.3.2.1: 29 Cross section view of the system model indicating the "z" gap.



z: distance from transmitter surface to receiver surface
 Coil-to-coil distance is larger than z.

4.2 Power Receiver Functional Block Diagram

4.2.1 System Model

4.2.1.1 System model PRx circuit topology

The system model PRx circuit topology is presented in Figure 5.2.1.1: 30 and in Table 5.2.1.1: 15 .

During digital ping and BPP mode S1 is open. After MPP handshake PTx will turn off and switch to 360kHz, when PRx detects 360kHz it will turn on S1 to enter MPP power delivery mode.

PRx comprises:

- Series impedance tuning network for BPP and MPP
- Parallel resonant for detection
- Ideal full-bridge rectifier

Additionally, the system model PRx the assumption that the load has a power converter (e.g. Buck converter) for converting between the optimal Vrect regulation voltage, to the 4V battery voltage. It has the following properties:

- The input current limit (Ilim) is controllable and used to control the maximum rectified power (see § 5.10.2.3 Ilim Loop (PRx)).
- The output voltage is regulated to battery voltage when Vrect > 4V

Figure 5.2.1.1: 30 System model PRx circuit topology (with BPP and MPP compatibility).

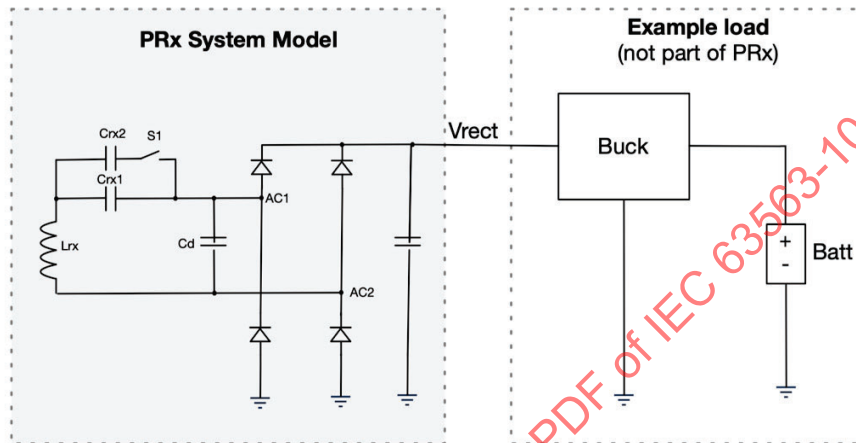


Table 5.2.1.1: 15 PRx series tuning configuration .

S1	Transmitter frequency	Power transfer mode
open	128kHz	128kHz digital ping
open	128kHz	BPP power transfer
closed	360kHz	MPP 360kHz digital ping and power transfer

4.2.1.2 System model PRx resonance tuning in BPP mode

Following the system model mechanical design in § 4.2 PTx Coil System Model , § 4.3 PRx Coil System Model and WPC v.1.2.4 part 1, spec 3.1.1, we can tune the BPP mode capacitors Crx1 to series resonant frequency:

$$f_s = \frac{1}{2\pi \cdot \sqrt{L'_{RX} \cdot C_{rx1}}} = 100 \text{ kHz} \pm 5\%$$

PRx coil inductance, mated with § 4.2 PTx Coil System Model in Qi frequency range:

$$L_{RX}' = 14.6 \mu\text{H}$$

So, the series resonant capacitor Crx1 is:

$$C_{rx1} = 174\text{nF}$$

In practical designs, the recommended tolerances of L_{rx}' and C_{rx1} are both $\pm 5\%$.

Parallel resonant frequency

$$f_p = \frac{1}{2\pi \cdot \sqrt{L_{RX} \left(\frac{1}{C_{rx1}} + \frac{1}{C_p} \right)}}$$

PRx coil inductance without PTx ferrite present (Free air inductance) L_{rx} :

$$L_{RX} = 9.17\mu\text{H}$$

So

$$C_d = 2.7\text{nF}$$

In practical designs, the recommended tolerance of L_{rx} is $\pm 0.6\mu\text{H}$, and C_d is $\pm 10\%$.

4.2.1.3 System model resonance tuning in MPP mode

Following the system model mechanical design in § 4.2 PTx Coil System Model and § 4.3 PRx Coil System Model, we select the PRx resonant capacitor to be the following value based the mated inductance:

$$C_{rx} = C_{rx1} + C_{rx2} = 710\text{nF}$$

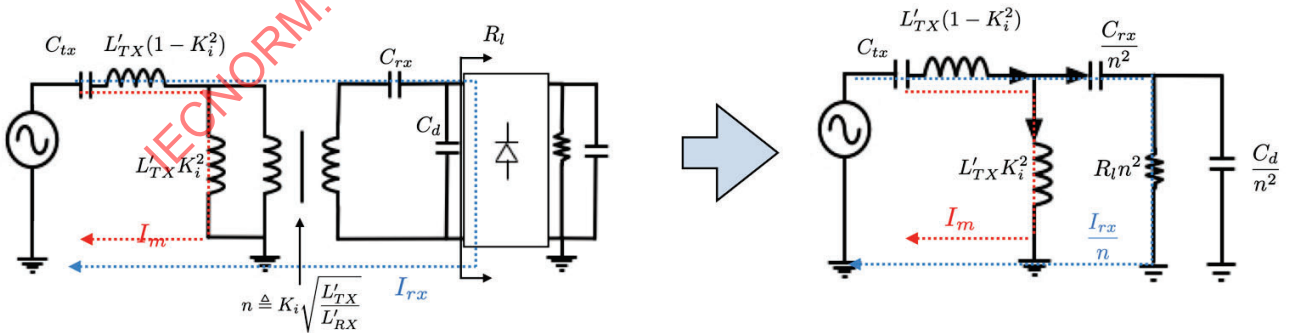
In practical designs, the observed tolerance of L'_{RX} is $\pm 1.55\mu\text{H}$ and C_{rx} is $\pm 10\%$.

Note that the C_{rx} value at 360kHz MPP mode is higher than C_{rx1} used for 128kHz BPP mode (174nF, see § 5.2.1.2 System model PRx resonance tuning in BPP mode), despite that the MPP frequency is higher. In BPP mode, C_{rx1} is chosen to tune the PRx coil to be close to the resonant point; this method works by minimizing the PRx reactance, and works well when the coupling is relatively low. When the coupling is high, as in the case with 360kHz MPP mode, C_{rx} needs to be chosen with C_{tx} considering PTx and PRx as a whole system, instead of just PRx in isolation. The following subsections explain the methodology of how C_{rx} and C_{tx} values are selected for the system model in MPP mode.

4.2.1.3.1 Rule of thumb

The rule of thumb in selecting resonant capacitor at 360kHz in the system model is to have its equivalent capacitance, including reflected C_{rx} , to resonant with the leakage inductance on the PTx side. Consider the Cantilever equivalent circuit in Figure 5.2.1.3.1: 31 :

Figure 5.2.1.3.1: 31 Cantilever Equivalent Circuit.



C_{tx} and C_{rx} should be selected so that the I_{rx} current branch (dotted blue) is close to resonance. The total equivalent capacitance is

$$C_{eq} = \frac{1}{\frac{1}{C_{tx}} + \frac{n^2}{C_{rx}}}$$

We have two different resonant frequencies:

1. Tx resonant frequency:

$$f_{tx} = \frac{1}{2\pi\sqrt{C_{tx}L'_{TX}}}$$

2. Power transfer resonant frequency:

$$f_r = \frac{1}{2\pi\sqrt{C_{eq}L'_{TX}(1-K_i^2)}}$$

And capacitors can be chosen correspondingly to tune the resonance points.

Since we are tuning the equivalent capacitance with regard to the leakage inductance, the C_{rx} value chosen in MPP mode is lower than C_{rx1} in BPP mode: the leakage inductance is much lower than the self-inductance, especially at high coupling locations.

Using the resonance equations only give an initial set of C_{tx} and C_{rx} values. The final values used in the system model are chosen with much more careful design considerations. Please see § 5.2.1.3.2 Selection of resonant capacitors .

4.2.1.3.2 Selection of resonant capacitors

In the system model, the resonant capacitors are selected to meet the following primary design goals:

- 15W power delivery within 2x2 cylinder;
- ZVS (zero voltage switching) is guaranteed for low EMI;
- Optimization for efficiency.

This section gives a summary of the design exercise leading to the selection of the capacitors in the system model.

Essentially, starting from the capacitor values indicated in § 5.2.1.3.1 Rule of thumb , there are three steps:

1. FHA (first harmonic approximation) to select initial capacitor values,
2. Time-domain sweeps of worst-case operating conditions to optimize the values,
3. Practical design considerations to finalize the values.

4.2.1.3.3 FHA analysis: selecting initial values of C_{tx}

The first step (FHA analysis) can be done analytically. The equivalent total input impedance at the transmitter side can be written as in eq. 1.

$$Z_{in}(s) = R'_{TX} + sL'_{TX} + \frac{1}{sC_{tx}} - \frac{Z_M^2}{\frac{R_l}{1+sC_dR_l} + sL'_{RX} + R'_{RX} + \frac{1}{sC_{rx}}} \quad \text{eq. 1}$$

where

- L'_{TX} , L'_{RX} , R'_{TX} , R'_{RX} are the mated PTx inductance, PRx inductance, PTx resistance and PRx resistance, respectively (see § 2.3.3 Symbols)
- C_d is the PRx parallel capacitor (see Figure 5.2.1.1: 30)
- Z_M is total mutual impedance. With inductive coupling K_i and resistance coupling K_r ,
 $Z_M \triangleq sK_i\sqrt{L'_{TX}L'_{RX}} + K_r\sqrt{R'_{TX}R'_{RX}}$
- R_l is the equivalent AC resistance of the load. In FHA, assuming the rectifier is in continuous conduction mode, it can be estimated as $\frac{8}{\pi^2} \cdot \frac{V_{rect}^2}{P_{rect}}$

Based on eq. 1, the system gain can be derived:

$$G(s) \triangleq \frac{V_{rect}}{V_{in}} = \frac{1}{Z_{in}(s)} \cdot \frac{Z_M R_l}{R_l + (1 + sC_d \cdot R_l) \left(R'_{RX} + sL'_{RX} + \frac{1}{sC_{rx}} \right)} \quad \text{eq. 2}$$

A valid set of resonant capacitor values should meet the following criteria for all possible magnetic parameters within the 2x2 cylinder:

1. The phase of $Z_{in}(s)$ (eq. 1) is less than 20 degrees to ensure ZVS
2. To reach the desired V_{rect} (14V, see Figure 5.2.1.5: 35) at 15W, the gain $G(s)$ (eq. 2) should be big enough such that the needed V_{in} that's less than the maximum (Table 5.3.1.3: 18)

On top of meeting 1 and 2, an optimized set of capacitor values should yield as high efficiency as possible.

The worst-case scenario of criteria 1 and 2 may be achieved at different operating conditions. For example, with all other parameters equal, the worst-case scenario of criterion 1 is reached at maximum K_l while the worst-case of criterion 2 is reached at minimum K_l .

A sweep of all operating conditions is then done to decide the best choice of C_{tx} and C_{rx} :

- Tuning C_{rx} to P_{RX} coil resonance leads to suboptimal C_{rx} values. A much higher C_{rx} is needed. This is evident by looking at the efficiency (Figure 5.2.1.3.3: 32), Z_{in} (Figure 5.2.1.3.3: 33) and gain (Figure 5.2.1.3.3: 34). This confirms the first principles shown in § 5.2.1.3.1 Rule of thumb .
- In the system model, a single selection of C_{tx} isn't possible to meet both criteria, so two different C_{tx} values are used depending on the range of K_l .

Figure 5.2.1.3.3: 32 Efficiency vs C_{rx} : sweep of C_{rx} at the maximum coupling position in the system model shows that efficiency is low when $C_{rx} < 300\text{nF}$ (system is capacitive) .

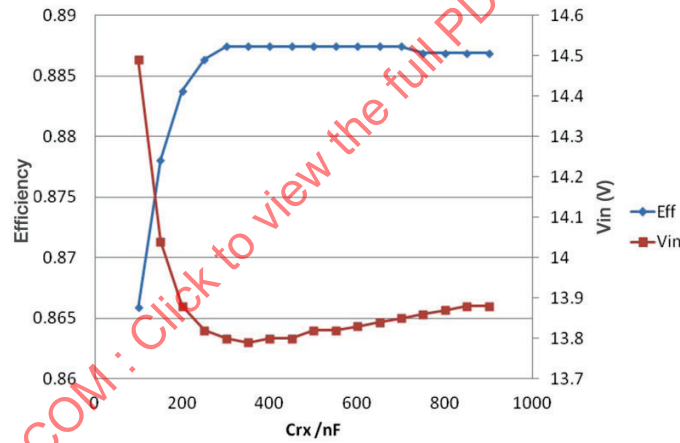


Figure 5.2.1.3.3: 33 Bode plot of $Z_{in}(s)$ at maximum coupling location with two different C_{rx} values. With $C_{rx}=60\text{nF}$, the system impedance is capacitive, which is undesirable.

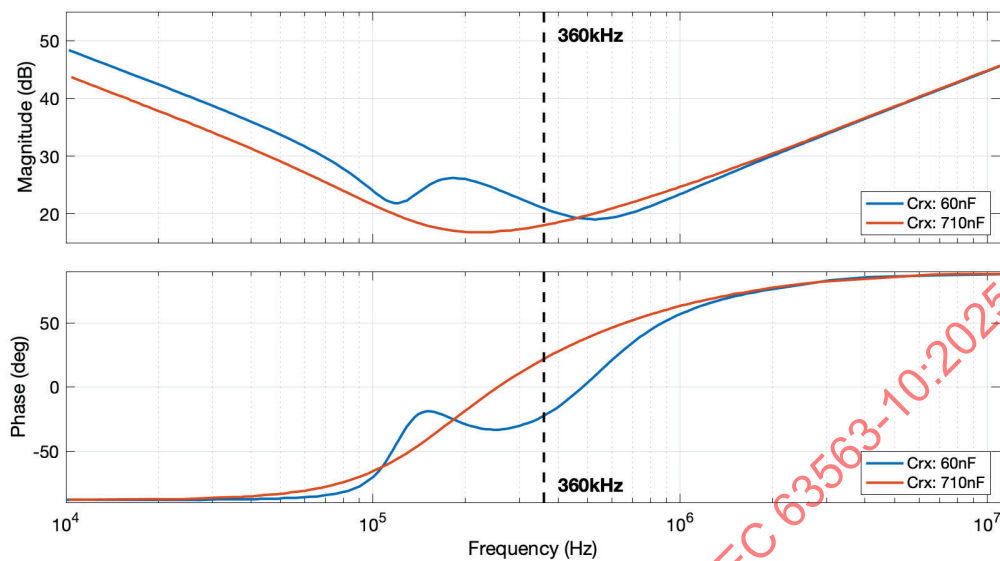
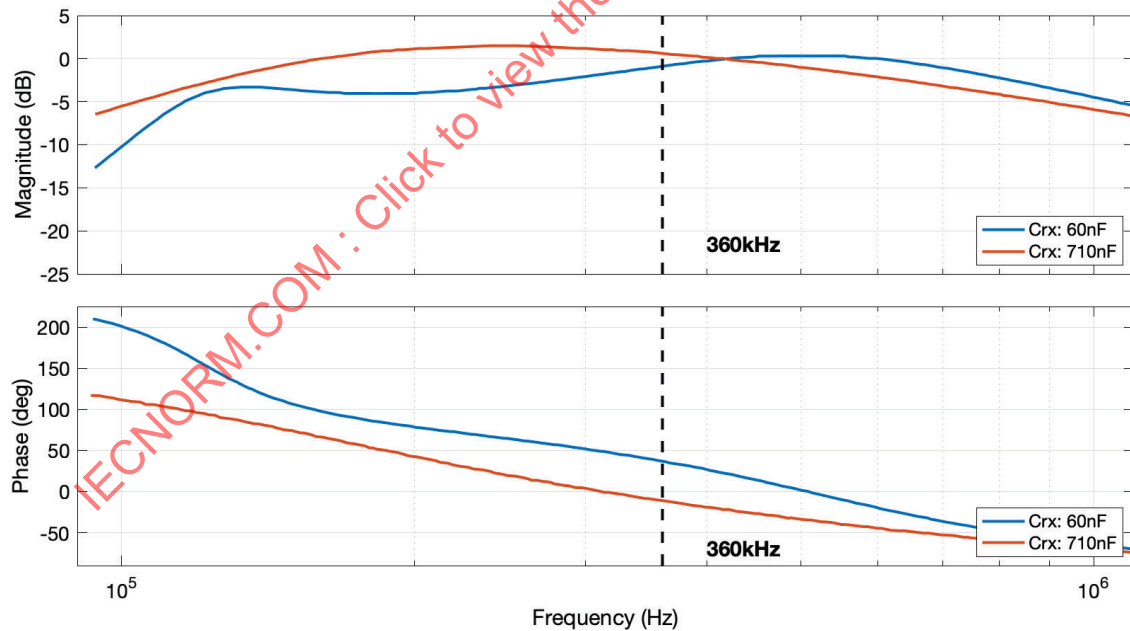


Figure 5.2.1.3.3: 34 Bode plot of $G(s)$ at maximum coupling location with two different C_{rx} values. $C_{rx}=710\text{nF}$ has $\sim 1.4\text{dB}$ higher gain than $C_{rx}=60\text{nF}$.



4.2.1.3.4 Time-domain sweep

Once the ranges of values of C_{tx} and C_{rx} capacitances are down selected, time-domain simulations are run to fine-tune the values. Time-domain simulations help to capture harmonic effects that are neglected in FHA. The third harmonic frequency is particularly impactful since it resonates with C_d , which is further explained in § 5.11 Mitigation of Side Effects of C_d at MPP Frequency .

4.2.1.3.5 Other design considerations

To determine the final values of the system-model C_{tx} and C_{rx} capacitance, there are a few other design considerations:

- With $C_{rx} \gg C_{tx}$, the tolerance on C_{rx} is reduced. This is very beneficial, as due to space limitations, PR_x usually has to use lower quality X5R capacitors (compared to C0G capacitors in the PT_x).
- With higher C_{rx} value and lower C_{tx} value, ASK modulation depth on V_{CTX} is increased.
- Capacitor values are rounded to the closest standard values. For example, the following table shows how C_{tx} values are rounded:

K_i range	Optimal equivalent C_{tx}	Final value
≥ 0.81	100nF	101nF (68nF + 33nF)
< 0.81	65nF	68nF

4.2.1.4 PR_x electrical properties

Table 5.2.1.4: 16 shows the electrical properties of the PR_x system model. Nominal values are from the system model, and min/max values represent recommended tolerances for practical designs.

Table 5.2.1.4: 16 PR_x electrical properties (system model).

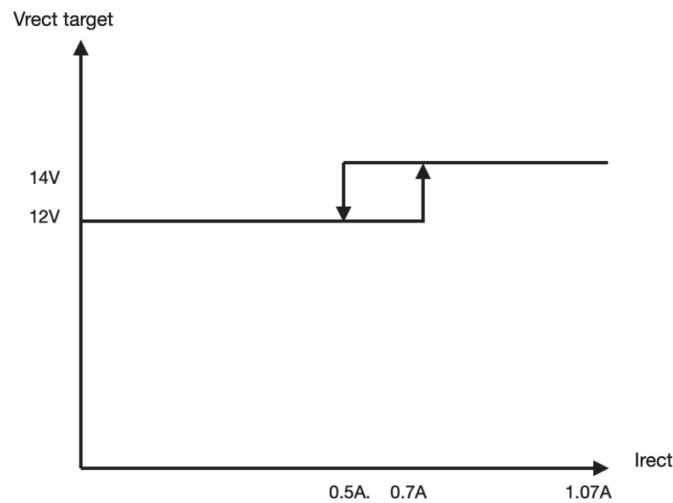
	<i>Min</i>	<i>Nominal</i>	<i>Max</i>
PR_x coil tuning capacitor $C_{rx1}+C_{rx2}$ MPP mode (Table 5.2.1.1: 15)	639nF	710nF	781nF
PR_x coil tuning capacitor C_{rx1} BPP mode (Table 5.2.1.1: 15)	156.6nF	174nF	191nF
Parallel capacitor C_d (including circuit parasitic capacitances)	2.43nF	2.7nF	3nF

4.2.1.5 System model PR_x V_{rect} setting

The intended rectified voltage regulation range of the system model PR_x is presented as an example in Figure 5.2.1.5: 35 .

- Rectified voltage target is selected based on I_{rect} (with hysteresis) for optimal wireless link efficiency and to limit max over voltage during load transients.
- The initial V_{rect} target is selected in § 5.9 Set Pr_max .

Figure 5.2.1.5: 35 System model PRx Vrect/Irect profile.



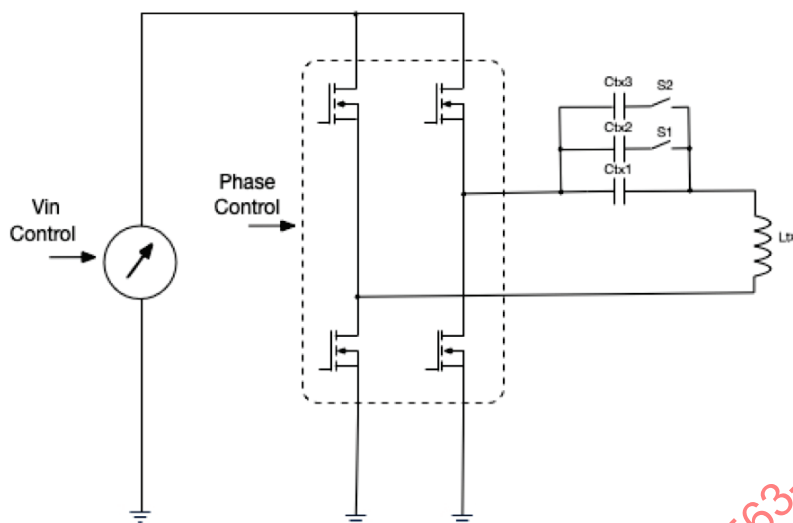
4.3 Power Transmitter Functional Block Diagram

4.3.1 System Model

Power transmitter power stage configuration is presented in Figure 5.3.1: 36 and in Table 5.3.1.2: 17 .

- In BPP mode and during 128kHz digital ping switches S1 and S2 are closed. See § 5.6 Digital Pings 128kHz/360kHz .
- After MPP handshake, starting with the 360kHz digital ping, PTx transfers to 360kHz operation mode and will select Ctx capacitor based on coupling estimation. Coupling estimation threshold, Ctx1 and Ctx2 are selected such that the phase delay between the voltage and phase fundamental tones is always higher than 20 degrees for inductive mode of operation and minimum power delivery is 15W inside 2mm cylinder. See § 5.7 K Estimation .
- The system model PTx employs full-bridge converter with input voltage control and phase-shift control to regulate transmitted power. Whenever possible, the system model PTx prefers voltage control over phase control. See § 5.10 Power Transfer Control .
- Operation frequency is fixed at 360kHz, with no variable frequency operation.
- Impedance tuning circuit comprising Ctx1, Ctx2, Cx3, S1 and S2 is controlled as described in Table 5.3.1.3: 18 .

Figure 5.3.1: 36 PTx power stage block diagram.



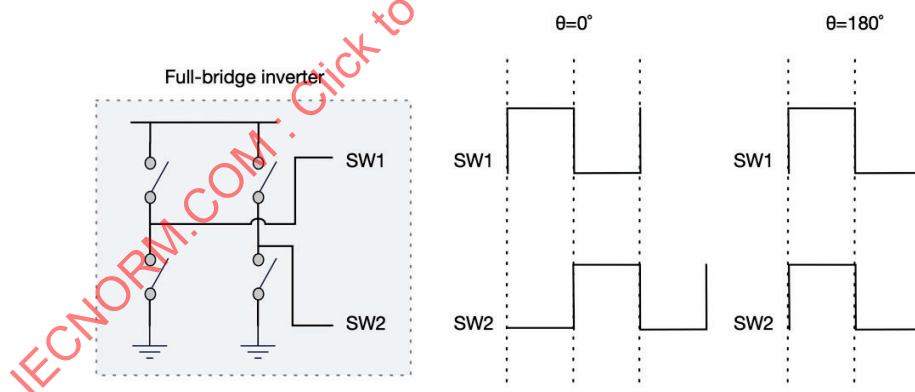
4.3.1.1 Definition of inverter phase θ

The inverter phase θ is defined as follows:

- when $\theta=0^\circ$, the effective output voltage of the full-bridge inverter is maximized
- when $\theta=180^\circ$, the effective output voltage of the full-bridge inverter is minimized (close to zero)

See Figure 5.3.1.1: 37 for an illustration of the definition of θ .

Figure 5.3.1.1: 37 Definition of inverter phase θ .



4.3.1.2 PTx resonant capacitor selection

In the system model, the PTx resonant capacitor is selected in conjunction with the PRx capacitor. Please see § 5.2.1.3 System model resonance tuning in MPP mode .

Table 5.3.1.2: 17 PTx power stage capacitor switches configuration.

<i>S1</i>	<i>S2</i>	<i>Transmitter frequency</i>	<i>Power transfer mode</i>
closed	closed	128kHz	Digital ping 128kHz and power transfer
open	open	360kHz	Digital ping 360kHz and power transfer (low coupling)
closed	open	360kHz	Digital ping 360kHz and power transfer (high coupling)

* "High" coupling and "low" coupling is determined by the k estimation stage (See § 5.7 K Estimation) which is performed in the digital ping phase. The value of k separating low and high coupling is given in the Table 5.3.1.3: 18.

4.3.1.3 PTx electrical properties

Table 5.3.1.3: 18 shows the PTx electrical properties of the system model. Notes:

- Tolerances are shown in brackets and are based on observations on a practical implementation of the system model;
- Values of all Ctx capacitors: Ctx1 = 68nF, Ctx2 = 33nF, Ctx3 = 390nF;
- $\alpha_{k_threshold}$ is read from the XID packet (see MPP communication protocol book). In the system model, $\alpha_{k_threshold}$ is a constant of 1.

Table 5.3.1.3: 18 PTx electrical properties (system model), during power transfer.

	<i>Value</i>
Input voltage range	11V-19V Capped at 18V in low-k mode (See § 5.9.2.3.4 Low-k Mode)
Amplitude modulation resolution	30mV
Duty cycle	50%
Max Vin with phase shift control	11V
θ (PTx inverter phase shift) control range	0- 50 degrees
θ (PTx inverter phase shift) control resolution	0.5 degrees
Primary coil tuning capacitor Ctx1+Ctx2 at high coupling $\geq 0.81 * \alpha_{k_threshold}$ (MPP mode, see Table 5.3.1.2: 17)	101nF (96-106nF)

Primary coil tuning capacitor Ctx1 at low coupling $< 0.81 * \alpha_k$ threshold (MPP mode, see Table 5.3.1.2: 17)	68nF (64.6-71.4nF)
Primary coil tuning capacitor Ctx1+Ctx2+Ctx3 (BPP mode, see Table 5.3.1.2: 17)	491nF (466.7-515.5nF)

4.4 Operating Frequency

4.4.1 System Model

The system model PTx uses a crystal oscillator and has a PWM clock frequency of 144MHz. The system model PTx also employs frequency dithering with 16 power cycles to reduce EMI.

In a practical design, PTx manufacturers can pick their clock frequency and optionally employ dithering with 2, 4, 8 or 16 cycles as long as the frequency specifications (§ 5.4.2 Specifications) are met. RCOs are generally not recommended as they won't meet the specifications.

4.4.2 Specifications

Section	Specification	Description
5.4.2.1	PTx Frequency Spec 1	The PTx operating frequency, when averaged over 16 consecutive cycles, shall be within $\pm 0.15\%$ of 360kHz.
5.4.2.2	PTx Frequency Spec 2	The PTx FSK modulated frequency F_{mod} , when measured and averaged over 16 consecutive cycles, shall be within $\pm 0.15\%$ of the nominal modulation frequency F_{mod} (see § 6.2 Frequency Shift Keying (PTx to PRx)).
5.4.2.3	PTX Frequency Dithering Spec 1	The PTx cycle periods, measured as T_1, \dots, T_{16} across 16 consecutive cycles, shall satisfy that $ 1/T_i - f < 10 \text{ kHz}$ for any $i=1, \dots, 16$, where f is 360kHz without FSK modulation or F_{mod} (see § 6.2 Frequency Shift Keying (PTx to PRx)) with FSK modulation.
5.4.2.4	PRX Frequency Dithering Spec 1	The PRx shall be capable of operating in MPP mode in the presence of PTx frequency dithering.

4.5 Object Detection

4.5.1 System Model

While power is applied to the PTx it will enter a low-power standby mode. In this mode, analog pings will be emitted periodically to detect the presence of a PRx. A simplified flow diagram (see Figure 7.2.1: 73) of the analog ping is shown in § 7.2 Open-air Q-Test (pre-power transfer FOD method) . It is not required to implement open-air Q test but the same flow diagram as well as the information presented about measuring Q and ping frequency (see § 7.2.6.1 Measuring Q) can be used as the basis for the analog ping.

In the object detection phase, the motion of the phone placement should be considered to prevent early detection of the placement (leading to, perhaps, k-estimation at an intermediate position) or false FO detection. These topics are considered in § 7.2.7 PRx movement and digital ping and § 7.2.6.4.2 PRx misplaced then replaced .

4.5.2 Specifications

Section	Specification	Description
5.5.2.1	PRx Q Deflection Spec 1	The PRx shall generate a Q-deflection (ΔQ) greater than 20% within the active area for the PRx to be detected. See eq. 3 for how Q deflection is calculated.

4.6 Digital Pings 128kHz/360kHz

4.6.1 Need For Digital Pings 128kHz / 360kHz

After object detection (See § 5.5 Object Detection) detects arrival of an object within its operating volume, the PTx does not yet know whether the arrived object is a valid PRx or a foreign object. The PRx may be completely out of energy - also known as dead battery. Even if the PRx is alive, it is not aware of being close to the PTx, as the PTx might have removed the power signal to conserve energy.

After the PTx determines that there may be a PRx within its operating volume, the PTx initiates a Digital Ping to initiate a response from the PRx.

In Figure 5.6.1: 38 , adopted from Figure 3.1 of MPP Communication Protocols Document Rev. 3.0 dated 08/19/2022, there are two sets of operations: (1) Digital Ping 128kHz and (2) Digital Ping 360kHz. See Figure 5.6.1: 39 .

Digital Ping 128kHz includes:

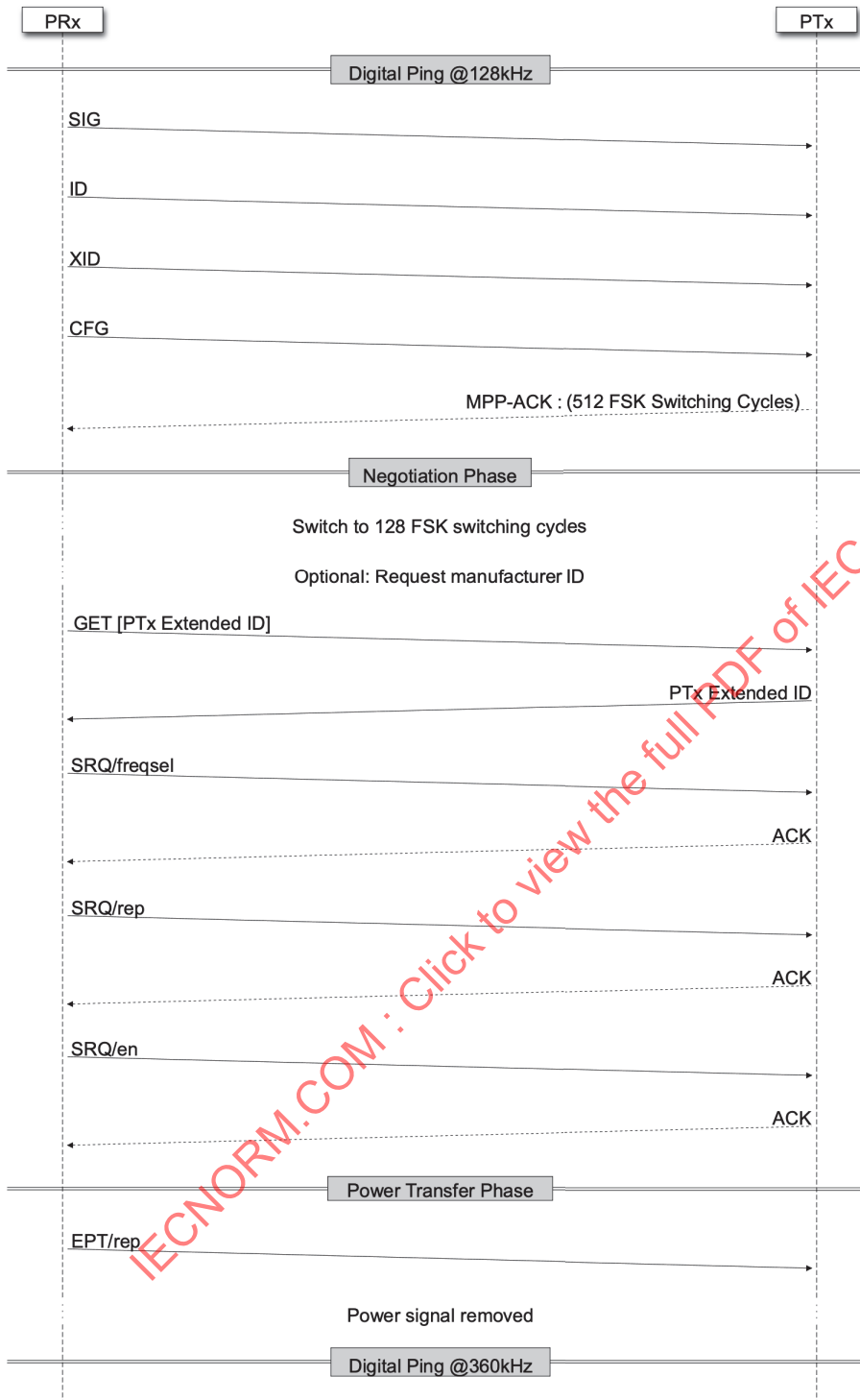
- "Digital Ping" phase, shown in Figure 5.6.1: 40
- "Identification 128kHz" phase, shown in Figure 5.6.1: 41 , and
- "Configuration" phase, shown in Figure 5.6.1: 43 .

Digital Ping 360kHz includes:

- "Digital Ping" phase, shown in Figure 5.6.1: 40
- "Identification 360Hz" phase, shown in Figure 5.6.1: 42 , and
- "Configuration" phase, shown in Figure 5.6.1: 43 .

Please note that the "Digital Ping" phase and the "Configuration" phase are the same between 128kHz and 360kHz.

Figure 5.6.1: 38 MPP Power Negotiation Flow.



In "Digital Ping" phase (Figure 5.6.1: 40):

- Inverter turns on and the duty ratio (or phase shift) is ramped up.
- PTx expects the first ASK packet.
- PTx handles scenarios such as no-packet arrival, invalid packet, and valid SIG or EPT packets.

The "Identification" phase is different between Digital Pings 128kHz / 360kHz:

In Digital Pings 128kHz, "Identification 128kHz" phase happens (Figure 5.6.1: 41).

- PTx expects the ID and XID packets.
- PTx makes decision based on different scenarios depending on the ID and XID.
- If needed, PTx performs k-estimation.
- PTx decides the next operation conditions for the inverter: frequency, phase, and inverter configuration.

In Digital Pings 360kHz, case, the "Identification 360kHz" phase happens (Figure 5.6.1: 42).

- PTx expects the ID and XID packets.
- PTx makes decision based on different scenarios depending on the ID and XID.
- PTx decides the next operation conditions for the inverter.

The "Configuration" phase (Figure 5.6.1: 43):

- PTx handles the cases with CFG, PCH and Proprietary packets.
- PTx adjusts the FSK parameters, if applicable.

IECNORM.COM : Click to view the full PDF of IEC 63563-10:2025

Figure 5.6.1: 39 Top-level diagram.

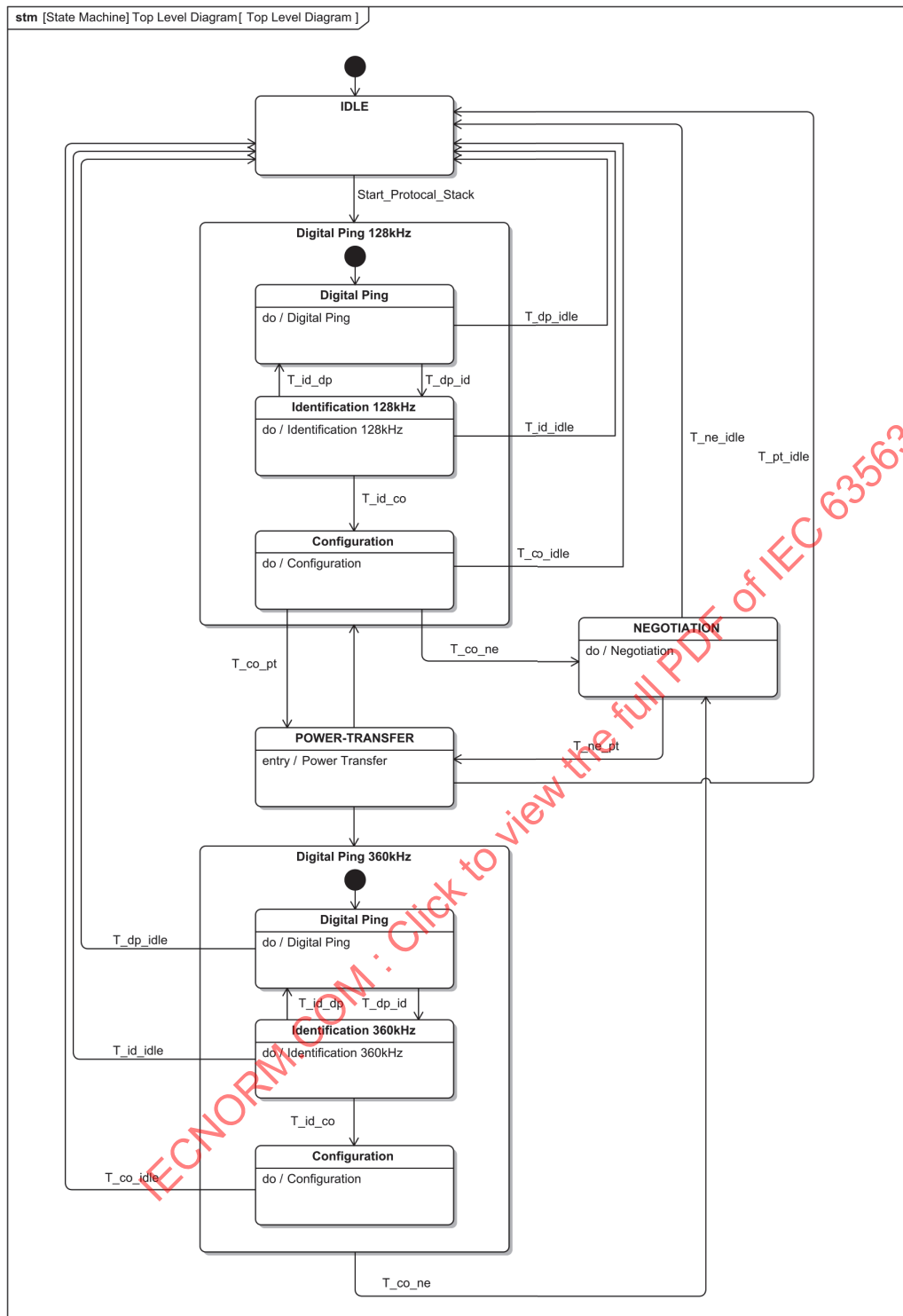


Figure 5.6.1: 40 Digital Ping Flowchart.

Inverter Operation Parameters are defined in subsequent sections.

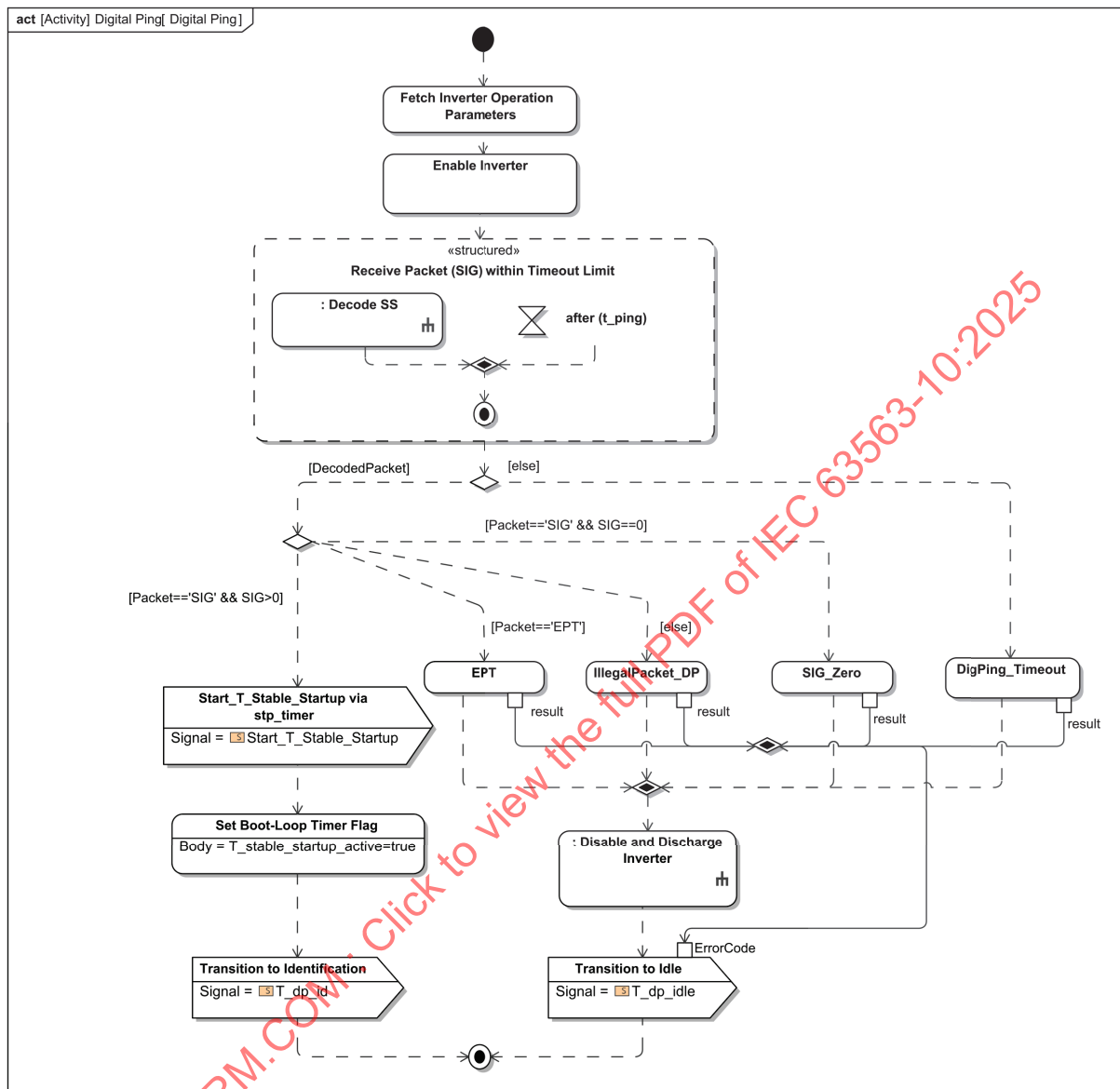


Figure 5.6.1: 41 Identification 128kHz Flowchart.

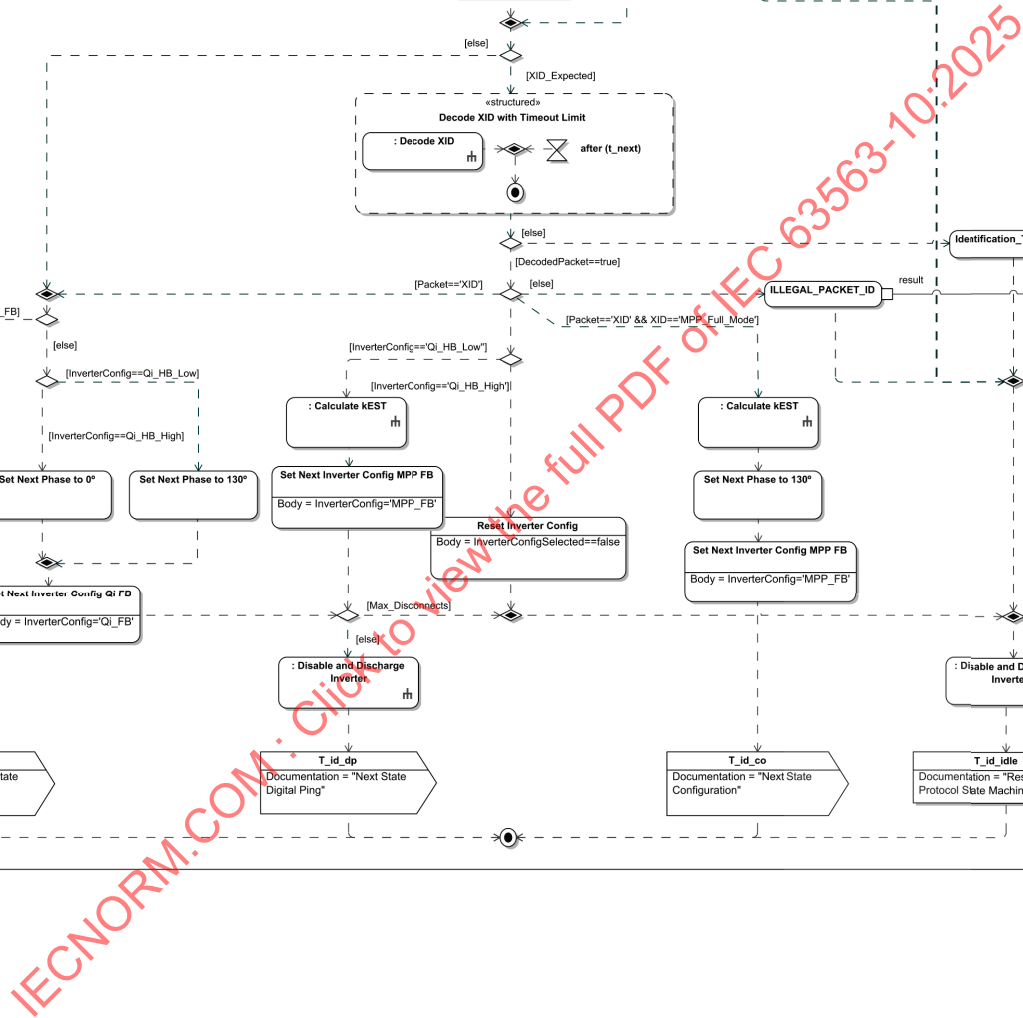


Figure 5.6.1: 42 Identification 360kHz Flowchart.

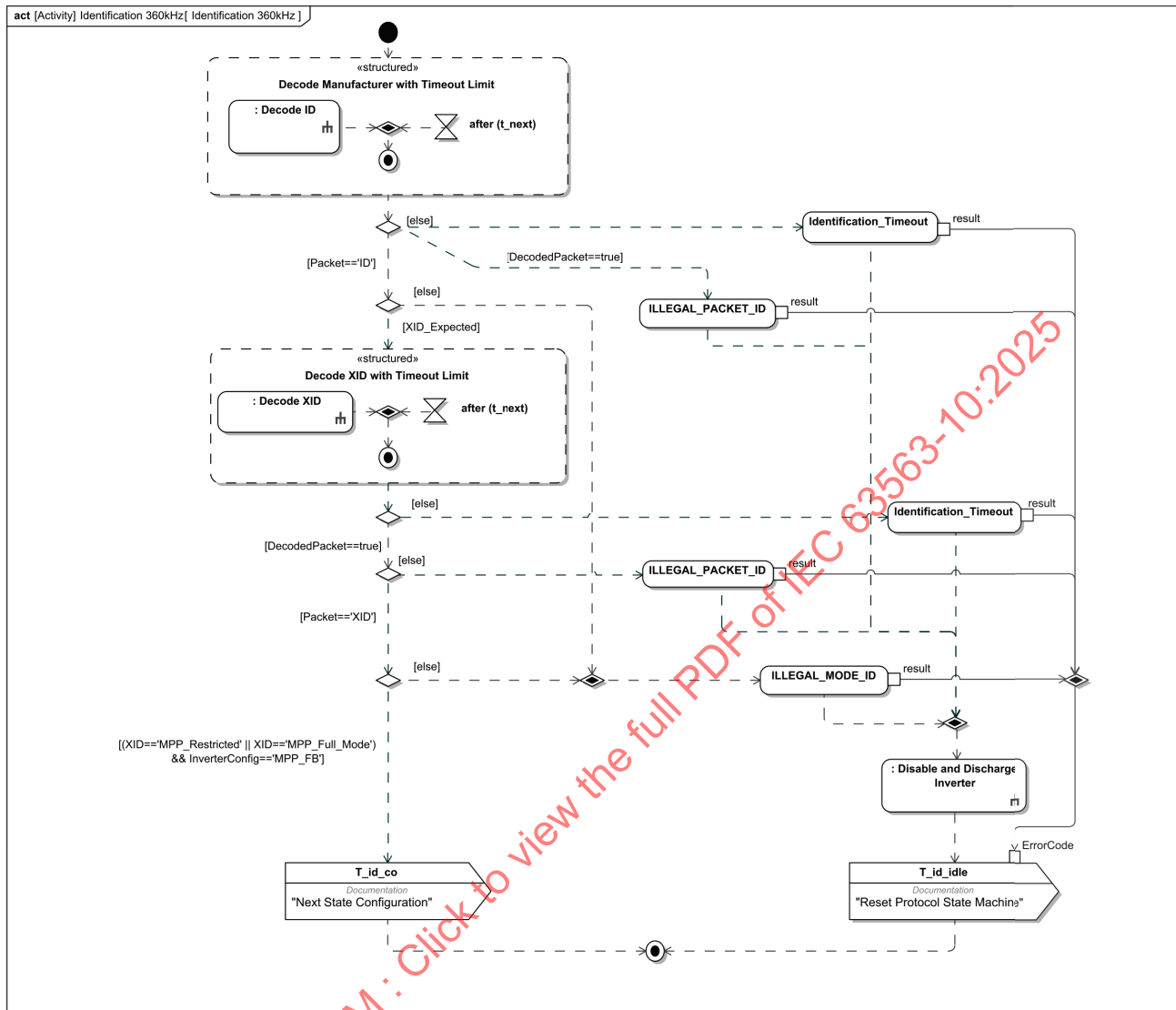
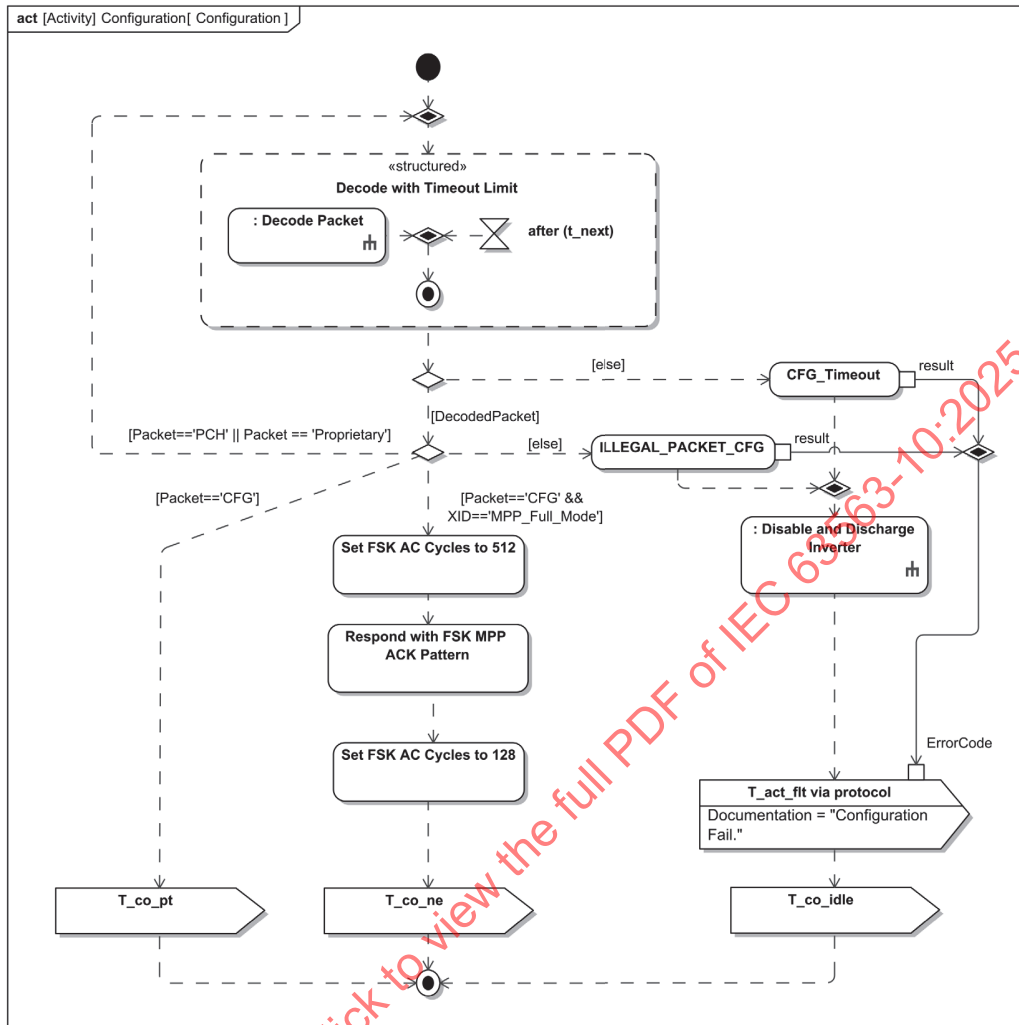


Figure 5.6.1: 43 Configuration Flowchart.



4.6.2 Specifications

4.6.2.1 PTx Digital Ping Specifications

There are four types of digital pings, separated by InverterConfig:

- 128kHz HB_Low Ping (InverterConfig == 'Qi_HB_Low')
- 128kHz HB_High Ping (InverterConfig == 'Qi_HB_High')
- 128kHz FB_High Ping (InverterConfig == 'Qi_FB')
- 360kHz FB Ping (InverterConfig == 'MPP_FB')

They are shown as different branches in Figure 5.6.1: 41 .

4.6.2.2 PTx Digital Ping Specifications - 128kHz Ping HB_Low

Section	Specification	Description
5.6.2.2.1	PTx DP 128kHz	PTx shall ensure its V_{inv} settles to 11.5V

Section	Specification	Description
	HB_Low Spec 1	
5.6.2.2.2	PTx DP 128kHz HB_Low Spec 2	PTx shall select the 491nF series resonant capacitor bank (shown in Figure 5.3.1: 36) according to Table 5.3.1.2: 17 .
5.6.2.2.3	PTx DP 128kHz HB_Low Spec 3	PTx shall start operation in half-bridge mode with $D=5\%$ and $f_{sw}=128\text{kHz}$.
5.6.2.2.4	PTx DP 128kHz HB_Low Spec 4	PTx ramps up D to 25% in 6msec and then keeps operating with $D=25\%$ for 65msec.
5.6.2.2.5	PTx DP 128kHz HB_Low Spec 5	PTx shall follow the flowchart in Figure 5.6.1: 41 .

4.6.2.3 PTx Digital Ping Specifications - 128kHz Ping HB_High

Section	Specification	Description
5.6.2.3.1	PTx DP 128kHz HB_High Spec 1	PTx shall ensure its V_{in} settles to 13V.
5.6.2.3.2	PTx DP 128kHz HB_High Spec 2	PTx shall select the 491nF series resonant capacitor bank (shown in Figure 5.3.1: 36) according to Table 5.3.1.2: 17 .
5.6.2.3.3	PTx DP 128kHz HB_High Spec 3	PTx shall start operation in half-bridge mode with $D=5\%$ and $f_{sw}=128\text{kHz}$.
5.6.2.3.4	PTx DP 128kHz HB_High Spec 4	PTx ramps up D to 50% in 6msec and then keeps operating with $D=50\%$ for 65msec.
5.6.2.3.5	PTx DP 128kHz HB_High Spec 5	PTx shall follow the flowchart in Figure 5.6.1: 41 .

4.6.2.4 PTx Digital Ping Specifications - 128kHz Ping FB

Section	Specification	Description
5.6.2.4.1	PTx DP 128kHz FB Spec 1	PTx shall ensure its V_{in} is stable at 11.5V.
5.6.2.4.2	PTx DP 128kHz FB Spec 2	PTx shall select the 491nF series resonant capacitor bank (shown in Figure 5.3.1: 36) according to Table 5.3.1.2: 17 .
5.6.2.4.3	PTx DP 128kHz FB Spec 3	PTx shall start operation in full-bridge mode with $D=50\%$ and $f_{sw}=128\text{kHz}$.
5.6.2.4.4	PTx DP 128kHz FB Spec 4	PTx ramps up phase shift in 6msec and then keeps operating for 65msec.
5.6.2.4.5	PTx DP 128kHz FB Spec 5	PTx shall follow the flowchart in Figure 5.6.1: 41 .

4.6.2.5 PTx Digital Ping Specifications - 360kHz Ping FB

Section	Specification	Description
5.6.2.5.1	PTx DP 360kHz FB Spec 1	PTx shall ensure its V_{in} is stable at 10V.
5.6.2.5.2	PTx DP 360kHz	PTx shall select the 68nF series resonant capacitor bank for low coupling Kest

Section	Specification	Description
	FB Spec 2	(shown in Figure 5.3.1: 36) according to Table 5.3.1.2: 17 .
5.6.2.5.3	PTx DP 360kHz FB Spec 3	PTx shall select the 101nF series resonant capacitor bank for high coupling (shown in Figure 5.3.1: 36) according to Table 5.3.1.2: 17 .
5.6.2.5.4	PTx DP 360kHz FB Spec 4	PTx shall start operation in full-bridge mode with $D=50\%$ and $f_{sw}=360\text{kHz}$.
5.6.2.5.5	PTx DP 360kHz FB Spec 5	PTx ramps the phase shift down to 0 degree with rate of 650 degrees/msec.
5.6.2.5.6	PTx DP 360kHz FB Spec 6	PTx shall follow the flowchart in Figure 5.6.1: 42 .

4.6.2.6 PRx Digital Ping Specifications

4.6.2.7 PRx Digital Ping Specifications

Section	Specification	Description
5.6.2.7.1	PRx DP Spec 1	MPP PRx shall apply $50\pm 5\text{mA}$ of current to V_{RECT} within 10ms after power signal is applied.
5.6.2.7.2	PRx DP Spec 2	The current shall be stable within 42-58mA with 29msec after power signal is applied.
5.6.2.7.3	PRx DP Spec 3	MPP PRx shall re-measures V_{RECT} with high precision starting 10ms after sending ID packet.
5.6.2.7.4	PRx DP Spec 4	MPP PRx shall measure high precision V_{RECT} for a period of 3ms.
5.6.2.7.5	PRx DP Spec 5	MPP PRx sends the high precision V_{RECT} value to PTx in XID packet (See MPP Communications Protocol Book, Section 7.1.22)

4.7 K Estimation

4.7.1 System Model

4.7.1.1 Need For K Estimation

In MPP systems, PTx and PRx collaboratively estimate the inductive coupling factor, K_i :

$$K_i = \frac{M'}{\sqrt{L_{TX}' L_{RX}'}}$$

where M' is the mutual inductance.

In MPP, the calculation of the estimated inductive coupling factor, K_{est} , takes place in PTx.

The potential use cases for K_{est} include:

1. Selection of C_{TX} for 360kHz operation (to deliver the full power and having ZVS)
2. Selection of proper PTx side slew-rate capacitors for EMI mitigation (both at light and heavy loads)
3. Prediction of deliverable power
4. Better selection of in-band communication parameters (e.g. a channel equalizer)
5. Selection of different ballast load for light-load OVP mitigation during load release.

Estimating K_i is a shared responsibility (see § 5.7.1.2 K_{est} Calculation Formula for definitions of the symbols used below):

PRx:

- informs PTx that it is of MPP type.
- selects proper timing (to ensure PTx has settled at 50% duty ratio) and then measures V_{rect} with high precision.

- sends the high precision V_{rect} value to PTx, in 20mV steps (see MPP Communications Protocol Book, Section 7.1.22)
- sends its specific α_{0rx} & α_{1rx} to PTx.

PTx:

- finds out that PRx is of MPP type.
- applies 50% duty ratio.
- measures V_{in} and V_{CTX_PP} with high precision.
- receives V_{rect} and α_{0rx} & α_{1rx} coefficients from PRx.
- Calculated p variable
- Calculates K_{est} by using stored E_{0xg} & E_{1xg} , received α_{0rx} & α_{1rx} coefficients from PRx, and calculated p variable.

4.7.1.2 Kest Calculation Formula

The equation to estimate K_i is as follows:

$$K_{est} = E_0 \cdot p + E_1$$

where:

$$p = \frac{V_{rect}}{V_{CTX_PP} + V_{in}}$$

V_{rect} : The Digital Ping voltage reported by RX

V_{in} : the measured dc voltage to the inverter

V_{CTX_PP} : is the measured peak to peak CTX voltage

The K_{est} formula is fit over a preferential k range from 0.72 to 0.88, i.e., E_0 and E_1 are chosen to be most accurate in this range. See § 5.7.1.2.1 E_0 and E_1 Fit Example for an example.

4.7.1.2.1 E_0 and E_1 Fit Example

Figure 5.7.1.2.1: 44 illustrates an example linear fit to calculate E_0 and E_1 . Figure 5.7.1.2.1: 45 shows how the data points are generated in simulation for this figure.

Figure 5.7.1.2.1: 44 E0 and E1 Fit Example.

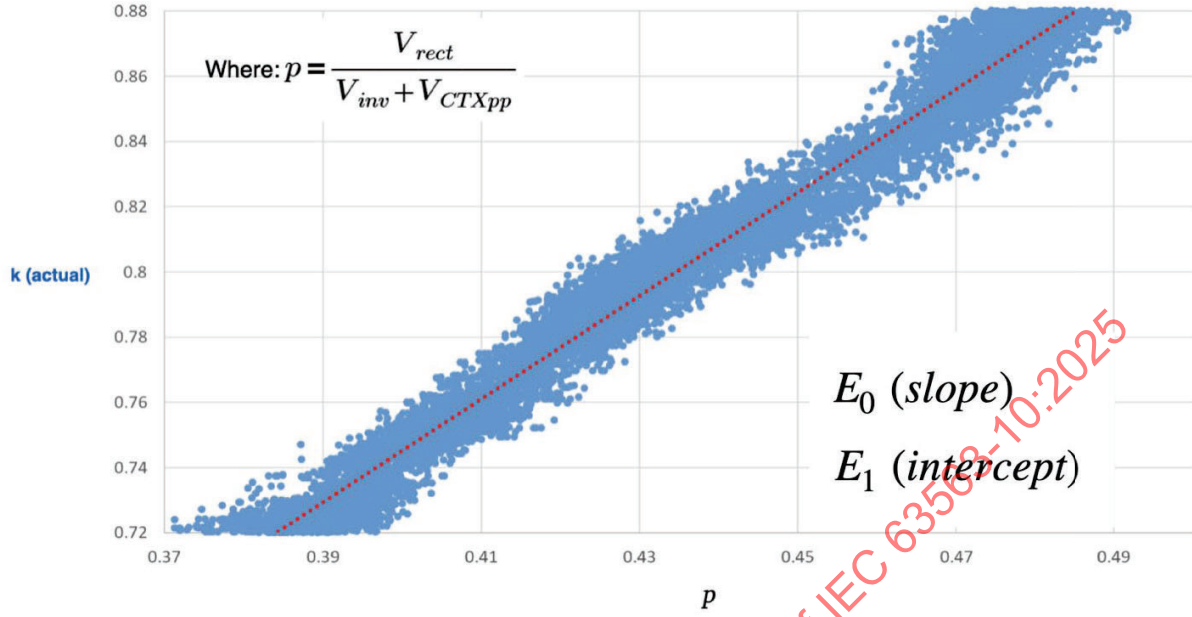
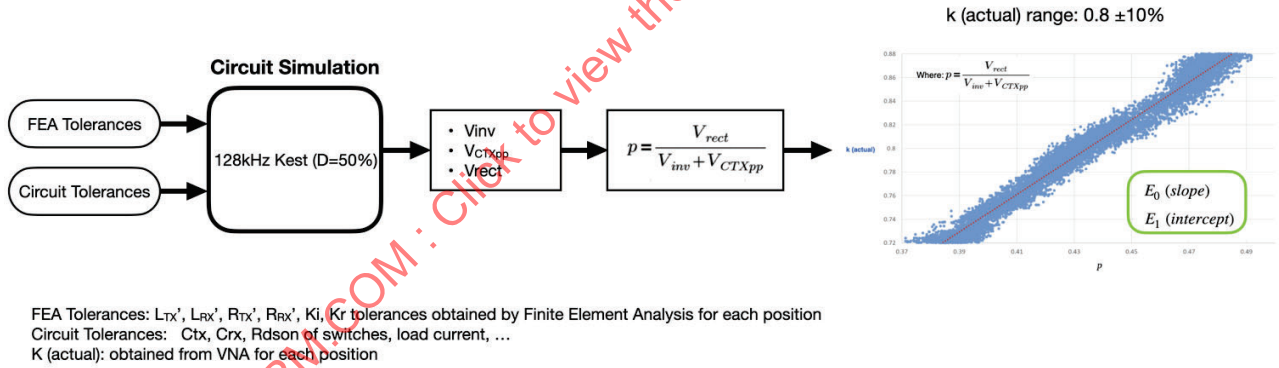


Figure 5.7.1.2.1: 45 Kest E0 and E1 Extraction Flow.



4.7.1.3 Eco-system Scaling

Section § 5.7.1.2 Kest Calculation Formula shows how we calculate Kest for a pair of PTx and PRx. In this section, we show how this formula is scaled to different PTx and PRx designs.

The base eigen fit coefficients E_{0xg} & E_{1xg} present the system-model PTx/PRx pair (see § 5.7.1.3.1 Subscript nomenclature for the nomenclature of subscripts used). To scale the parameters to allow different PTx and PRx designs, the scaled Kest formula is as follows:

$$Kest = E_{0xg} \cdot \alpha_{0rx} \cdot p + E_{1xg} \cdot \alpha_{1rx}$$

The assumption is: if for each position an PRx show higher coupling to the system-model PTx compared to the system-model PRx, then it is going to have higher coupling to any PTx compared with the system-model PRx; and the effect is proportional.

For more information see § 5.7.1.3.2 Calculation of Kest Scaling Factors .

4.7.1.3.1 Subscript nomenclature

Eigen Coefficient $E_{\{a\}\{b\}\{c\}}$:

- a: {0 or 1}
 - 0: the slope of linear curve fit
 - 1: the intercept of linear curve fit
- b: PTx. "g" means the system-model PTx (TPT#MPP1) and "x" means a general PTx.
- c: PRx. "g" means the system-model PRx (TPR#MPP1) and "y" means a general PRx.

Scaling factor $\alpha_{\{d\}rx}$:

d: {0 or 1}

- 0: the slope of linear curve fit
- 1: the intercept of linear curve fit

4.7.1.3.2 Calculation of Kest Scaling Factors

For a PRx, the Kest alpha scaling factors are obtained by getting the slope (E_0) and intercept (E_1) of the PRx and TPT. This set of coefficients are named eigen coefficients of TPT#MPP1 (subscript: g) vs PRx (subscript: y) E_{0gy} and E_{1gy} , respectively.

α_{rx} for PRx are calculated by the following equations:

$$\alpha_{0rx} = E_{0gy} / E_{0gg}$$

$$\alpha_{1rx} = E_{1gy} / E_{1gg}$$

where, $E_{0gg}=1.5926$, $E_{1gg}=0.1043$ which are eigen coefficients of TPT#MPP1 (g) vs TPR#MPP1 (g).

α_{0rx} and α_{1rx} are encoded in the XID packet (see MPP Communications Protocol Book, Section 7.1.22) and sent to PTx.

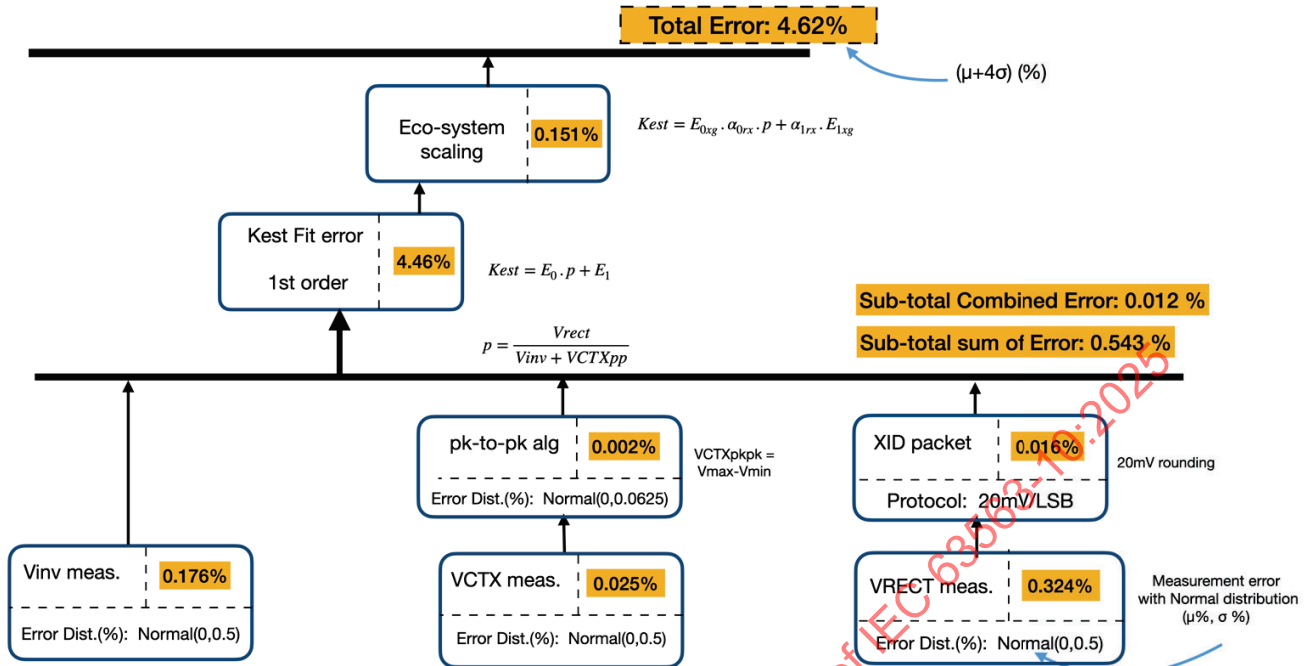
For a new PTx new eigen coefficients E_{0xg} and E_{1xg} are obtained by finding the slope (E_0) and intercept (E_1) of new PTx vs TPR#MPP1 and stored in non-volatile memory of PTx.

See § 5.7.1.2.1 E_0 and E_1 Fit Example for obtaining eigen coefficients for TX and RX pair.

4.7.1.4 Error stack-up

The Kest process is sensitive to errors. § 5.7.1.4 Error stack-up demonstrates the error stack-up for an example PTx/PRx pair for Kest.

Figure 5.7.1.4: 46 Example PTx/PRx Kest Error Stack-up.



4.7.2 Specifications

Section	Specification	Description
5.7.2.0.1	PTx KEST Spec 1	MPP PTx unit shall know its specific eigen coefficients of PTx vs TPR which are named E_{0xg} and E_{1xg} . E_{0xg} and E_{1xg} are characterized by testing PTx on the test receiver that implements the system model PRx (TPR), and stored in PTx nonvolatile memory.
5.7.2.0.2	PTx KEST Spec 2	MPP PTx unit shall increase the duty ratio from 25% to 50% within 1ms after reception of ID packet (header 0x71), if not already at 50%.
5.7.2.0.3	PTx KEST Spec 3	MPP PTx unit shall measure the inverter DC voltage, V_{inv} with $4\sigma \leq 2\%$ after duty ratio has settle down to 50%.
5.7.2.0.4	PTx KEST Spec 4	MPP PTx unit shall measure the peak-peak voltage across the compensating capacitor CTX, V_{CTX_PP} , with high precision ($4\sigma \leq 2\%$) after duty ratio has settle down to 50%.
5.7.2.0.5	PTx KEST Spec 5	MPP PTx unit shall extract the V_{rect} and α_{0rx} and α_{1rx} coefficients from XID packet (header 0x81).
5.7.2.0.6	PTx KEST Spec 6	MPP PTx unit shall calculate: $Kest = E_{0xg} \cdot \alpha_{0rx} \cdot \frac{V_{rect}}{V_{CTX_PP} + V_{inv}} + E_{1xg} \cdot \alpha_{1rx}$
Section	Specification	Description
5.7.2.0.7	PRx KEST Spec 1	MPP PRx unit shall know its specific coefficients α_{0rx} and α_{1rx} . α_{0rx} and α_{1rx} are characterized by testing PRx on the test transmitter that implements the system model (TPT) and stored in PRx nonvolatile memory.
5.7.2.0.8	PRx KEST Spec 2	PRx shall wake up when V_{rect} exceeds $V_{rect} - WakeUp - Threshold$.

Section	Specification	Description
		$V_{rect - WakeUp - Threshold}$ is 3.5V.
5.7.2.0.9	PRx KEST Spec 3	PRx shall send ID packet (header 0x71).
5.7.2.0.10	PRx KEST Spec 4	The PTx shall measure Vrect within 2ms before sending XID packet. Note: VRECT value is in 20 mV units as defined in MPP Communications Protocol Book, Section 7.1.22.
5.7.2.0.11	PRx KEST Spec 5	The PRx shall send its measured VRECT, α_{0rx} and α_{1rx} coefficients in the XID packet. Note: Vrect is in 20mV units and coefficients α_{0rx} and α_{1rx} are encoded as signed 8-bit fields as shown in the XID packet definition in MPP Communications Protocol Book, Section 7.1.22.

4.8 Output Impedance and Load Transients

4.8.1 System Model

4.8.1.1 Slope of the output Impedance

Figure 5.8.1.1: 47 shows a typical plot of the relationship between Vrect and Irect, with regard to fixed Vin and θ . We can see the Vrect vs Irect is almost a straight line for each Vin and θ combination. Specifically, this means that we can write their relationship as

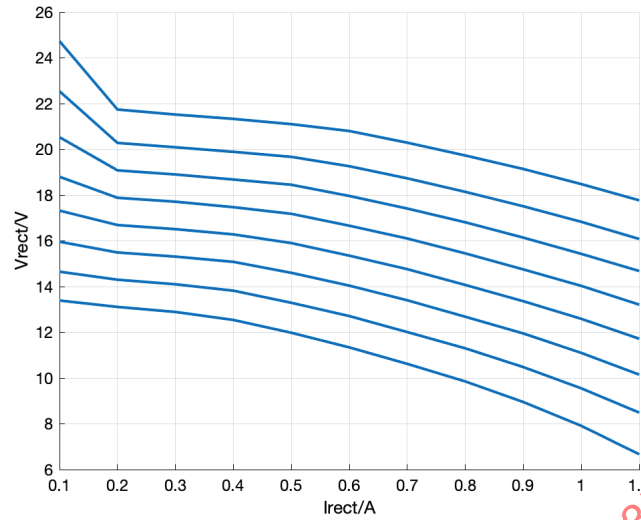
$$V_{rect} = a \cdot I_{rect} + b$$

where a is the slope of the linear line. So we can use the concept of *slope* to describe the output impedance. Specifically, a *steep* output impedance means that with a small change of Irect, we can observe a big change in Vrect. In general, we would like to avoid a steep output impedance, because it increases the risk of power disconnect and termination via:

- receiver over-voltage in the event of load release,
- receiver brown-out in the event of load increase, and
- control instability in general.

Therefore, we could use load step/dump procedures to verify that the slope of output impedance is within acceptable limits (See an example in § 5.8.1.2 Worst-case tests to measure the slope of the output impedance).

Figure 5.8.1.1: 47 Typical Output Impedance Plot (V_{rect} vs I_{rect}) .



Note: 1) Each line represents fixed V_{in} voltage and θ ; 2) the initial steep slope is caused by 3rd harmonic resonance with C_d (see § 5.11 Mitigation of Side Effects of C_d at MPP Frequency)

4.8.1.2 Worst-case tests to measure the slope of the output impedance

When designing an MPP PTx, it's important to measure the slope of the output impedance. MPP PTx designers can refer to the following load step procedure (§ 5.8.1.2.1 Load step procedure) and load dump procedure (§ 5.8.1.2.2 Load dump procedure) to create worst-case test scenarios to test the load step of their designs.

4.8.1.2.1 Load step procedure

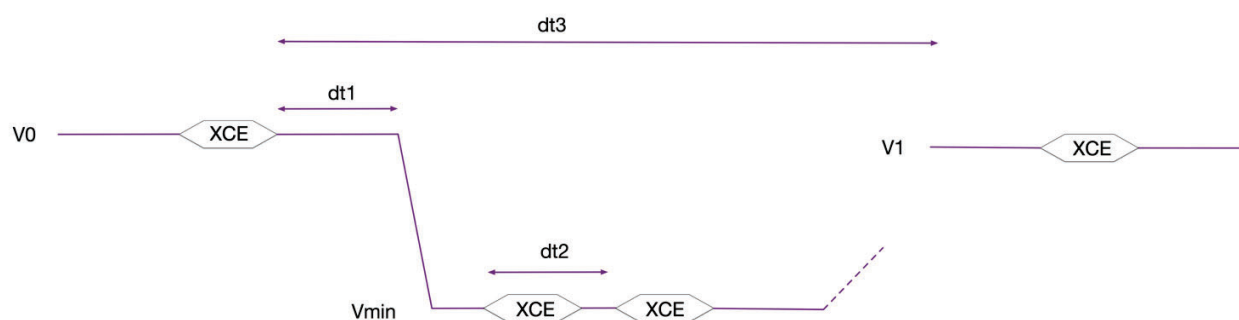
The following procedure can be used to measure an MPP PTx's slope of output impedance at a worst-case load step event:

1. Place system model PRx on the system model PTx to position $X=3$ mm, $Y=3$ mm, $Z=3$ mm
2. The PTx should be set in MPP low coupling mode (S_1 open S_2 open, see Table 5.3.1.2: 17)
3. Set initial load to 50mA
4. Establish communication and set V_{rect} target to 15V $\pm 0.5V$, with 560ms interval between consecutive XCE packets
5. Change the load to 550mA $dt_1 = 50$ ms after sending XCE packet as presented in Figure 5.8.1.2.1: 48
6. Monitor that PRx continues to regulate V_{rect} by sending error packets at the rate of $dt_2=80$ ms and PTx responds to XCE packets by increasing V_{in} / decreasing phase (i.e, increasing equivalent V_{inv} as defined in § 5.9.4.1)
7. Measure rectified voltage reaches regulation point within $dt_3=2$ s

The V_{rect} voltage in the system model is:

V_{rect}	Value
V0	14.5-15.5V
Vmin	7V
V1	14.5-15.5V

Figure 5.8.1.2.1: 48 Vrect timing diagram during load step procedure in the system model .



4.8.1.2.2 Load dump procedure

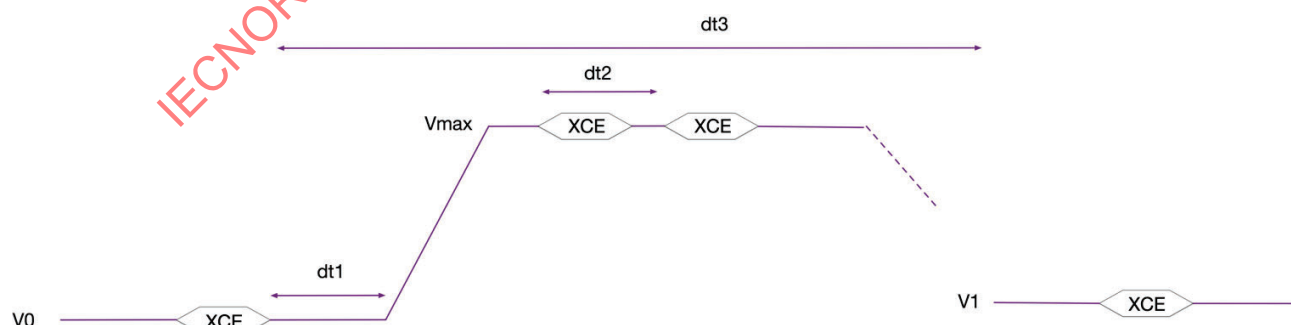
The following procedure can be used to measure an MPP PTx's slope of output impedance at a worst-case load dump event:

1. Place system model PRx on the system model PTx to position X=0mm, Y=0mm, Z=1mm
2. The PTx should be set in MPP high coupling mode (S1 closed S2 open, see Table 5.3.1.2: 17)
3. Set initial load to 580mA as presented in Figure 5.8.1.2.2: 49
4. Establish communication and set Vrect target to 12V +/-0.25V, with 560ms interval between consecutive XCE packets
5. Change the load to 100mA dt1 = 50ms after sending XCE packet
6. Monitor that PRx continues to regulate Vrect by sending error packets at the rate of dt2=80ms and transmitter responds to XCE packets by decreasing Vin / increasing phase (i.e. decreasing equivalent Vinv as defined in § 5.9.4.1)
7. Measure rectified voltage reaches regulation point within dt3=2s

The Vrect voltage in the system model is:

Vrect	Value
V0	11.75-12.25V
Vmax	19V
V1	14.25-15.75V

Figure 5.8.1.2.2: 49 Vrect timing diagram during load dump procedure in the system model .



4.9 Set Pr_max

4.9.1 Background

Set Pr_max is an optional stage in the MPP protocol that aims to aid the PTx and PRx pair to find its best operating point. It occurs after the PRx has been identified as an MPP receiver, and at the beginning of the MPP power transfer stage before the PRx delivers power to its system load. It is used in the system model for PRx to find its initial Vrect target and maximum Prect that satisfy the needs of both PTx and PRx. The Vrect target set by this stage is an initial value. Afterward, Vrect target can change. The system model updates its Vrect target according to Figure 5.2.1.5: 35 .

This stage helps the system model PRx to:

- recognize the power-stage gain at the current coupling position; and consequently,
- select an operating point that may have a higher efficiency, better control-loop stability, and/or lower risk of over-voltage;

Accordingly, the remaining sections are organized in the following way:

- § 5.9.2 System Model : describes how the system model sets Pr_max;
- § 5.9.3 PTx Specifications : contains requirement specifications that any MPP PTx shall meet in the case when a mated PRx performs the procedure to set Pr_max.

4.9.2 System Model

4.9.2.1 Theory of Operation

System model PRx uses power contract to decide on the initial values of

1. Vrect_target: the target Vrect voltage to run the § 5.10.2.2 Vrect_target Loop (PRx+PTx) against.
2. Pr_max: the maximum rectified power that the PRx can draw.

To set both values, a good indicator of the current operating point for PRx is the power-stage gain G. Specifically, G can be defined as the ratio of two end-to-end dc voltages, i.e.

$$G = \frac{V_{rect}}{V_{inv}}$$

where Vrect is the PRx rectified voltage, and Vinv is the equivalent dc input voltage (See § 5.9.4.1). A bigger G indicates a higher power gain and potentially a more strongly-coupled inductive link, but also indicates that it's easier for the control loop to overshoot.

Most of the power contract flow is to measure G. Since G is dependent on the PRx load and PTx input voltage, and it would be impractical to sweep all loads and voltages. In practice, we measure two gains: G1 and G2, under two different load conditions. The final decision is based on both Gs, or whichever is available. i.e., the G1 and G2 we are measuring are:

$$G_1 = \left. \frac{V_{rect}}{V_{inv}} \right|_{\text{light load}} \quad G_2 = \left. \frac{V_{rect}}{V_{inv}} \right|_{\text{mid load}}$$

4.9.2.2 PRx ballast current

During the digital ping sequence, a 50mA load current is required on the PRx (§ 5.6.2.7.1). The system model PRx implements this as a "ballast current" that's directly applied to the dc nodes of the rectifier. This ballast current is present during power transfer as well, and has the following properties:

- If the load (e.g., battery with a battery charger) is not connected, or is connected but with very low current (<50mA), then the ballast current is in effect and rounds the total equivalent dc current up to 50mA;
- If the load is connected and is drawing more than 50mA, then the ballast current is not effective.

During the Set Pr_max flow, the PRx will

1. start with no load connected and a 50mA ballast load, and then,
2. connect the load and set a 400mA load limit for the load to ramp up.

G1 and G2 are measured under these two different load conditions. If we run into any failure, we'll set the operating point to the "safe mode" with $V_{rect_target} = 12V$ and $Pr_{max} = 5W$.

At the end of the Set Pr_{max} flow, the load is already connected, so the PRx can smoothly transit to power transfer mode.

4.9.2.3 Set Pr_{max} Flow

Based on § 5.9.2.1 Theory of Operation , System model PRx power contract follows the following flow:

IECNORM.COM : Click to view the full PDF of IEC 63563-10:2025

4.9.2.3.1 Overall Flow

Figure 5.9.2.3.1: 50 Set Pr_max Overall Flow .

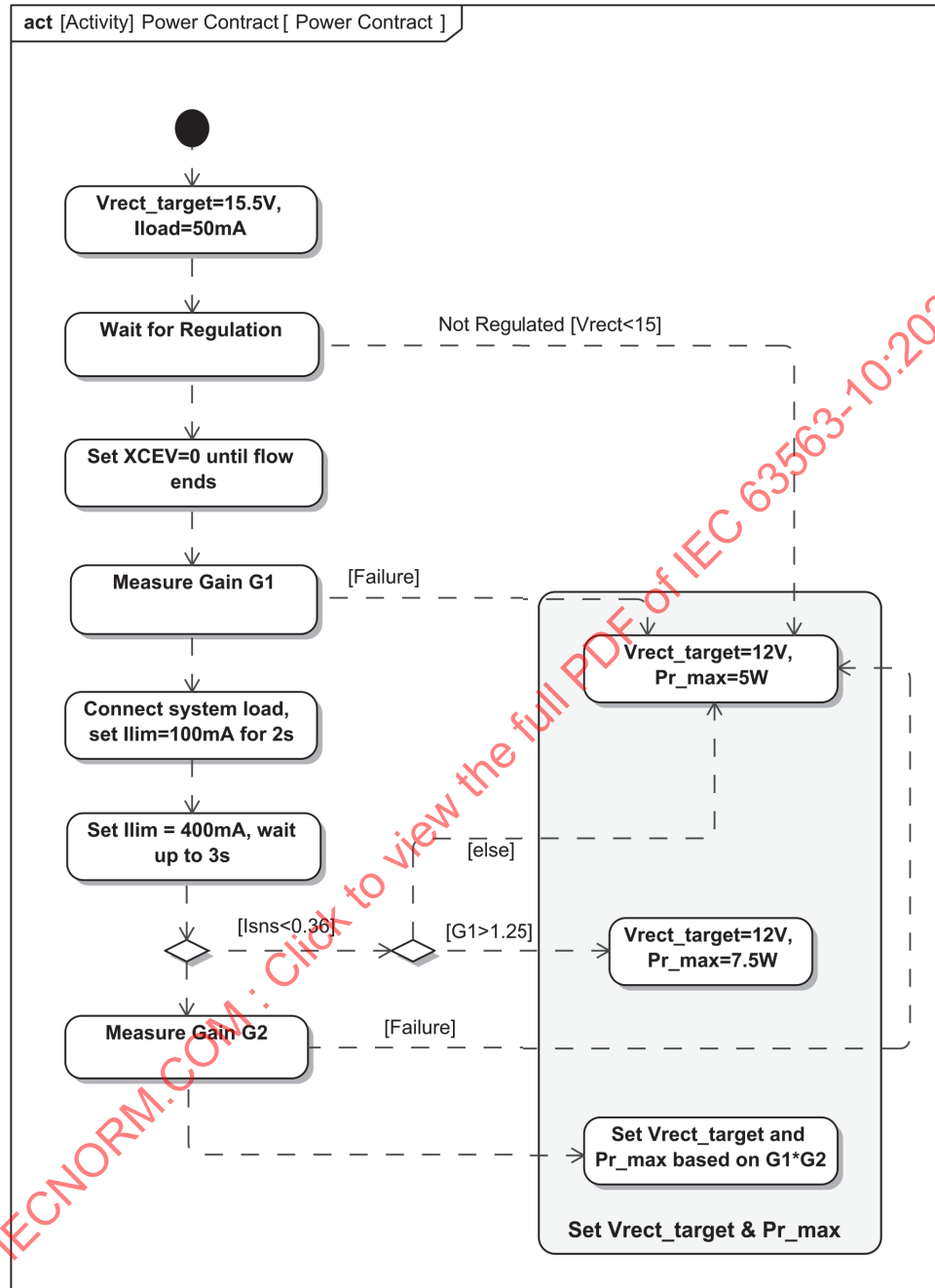
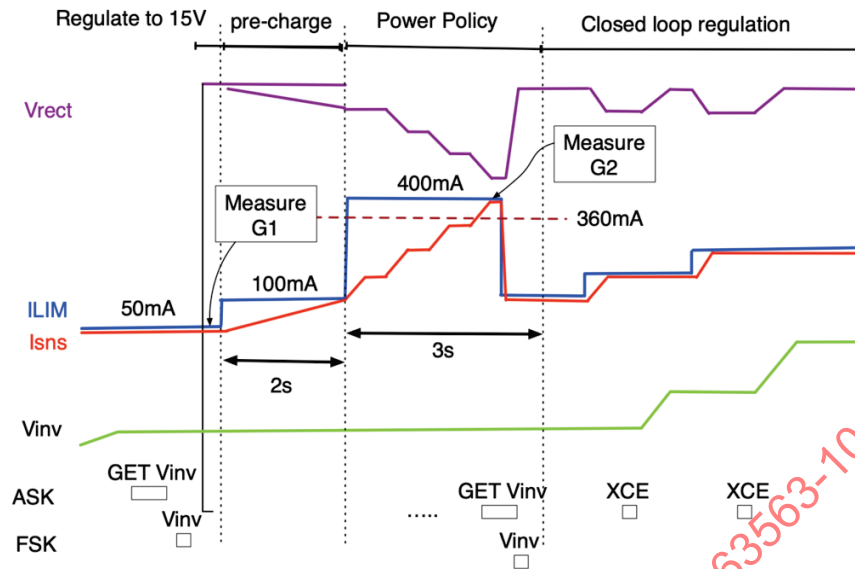


Figure 5.9.2.3.1: 51 Example Time Sequence .



Note: In the time sequence example diagram:

- I_{lim} is the load current limit and I_{sns} is the sensed load current.
- The ramp-up steps in I_{sns} are caused by practical limitations on how fast the load current can ramp up.
- The drop of I_{lim} and I_{sns} at the beginning of the closed-loop regulation is typical and is caused by the anti-crash scheme in I_{lim} control loop (see § 5.10.2.3.2 I_{lim} Freeze and Anti-Crash Mechanism).

4.9.2.3.2 Gain Measurement

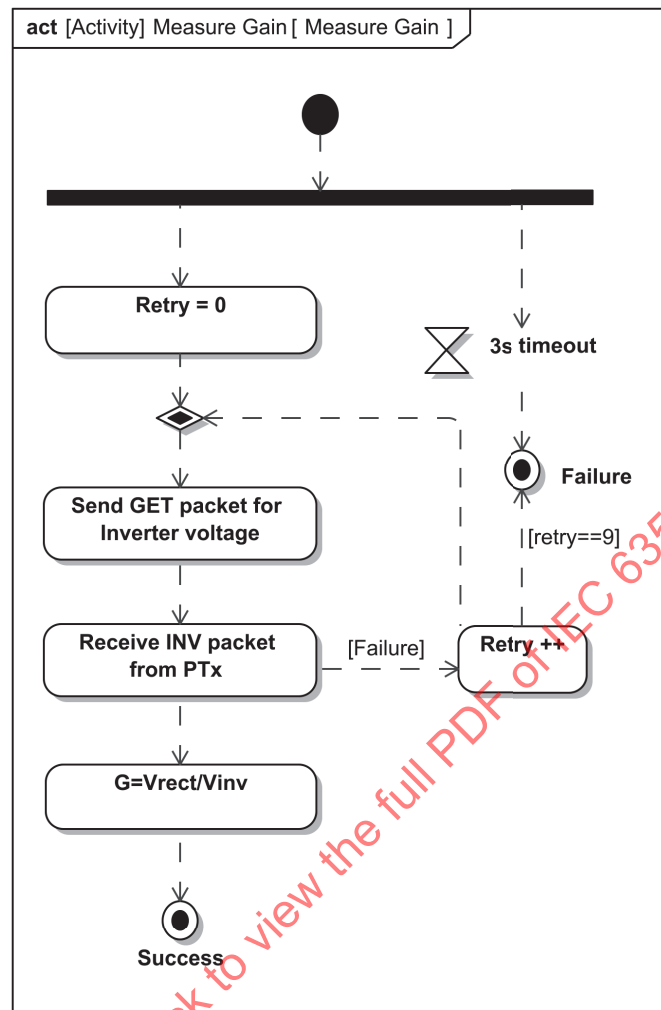
The "Measure Gain" block in the overall flowchart is the same for G1 and G2.

System model utilizes the GET ASK packet and INV FSK packet from MPP Communication Protocols to obtain equivalent inverter voltage V_{inv} from PTx (see § 5.9.4.1). There are two possible ways that this flow can fail:

1. PRx tries reaches maximum and still cannot get a valid INV packet from PTx, or
2. The overall flow takes more than 3 seconds.

If gain measurement fails, we'll follow the failure branch in the overall flow.

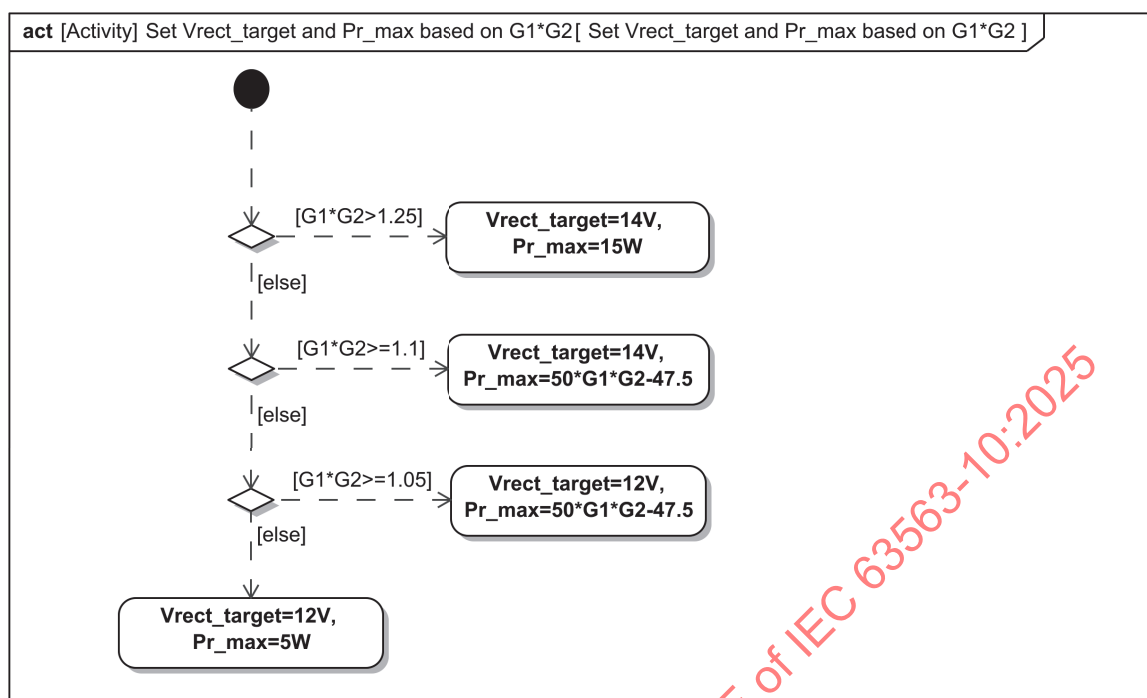
Figure 5.9.2.3.2: 52 Gain Measurement Flow .



4.9.2.3.3 Setting initial V_{rect_target} and Pr_max based on $G1 \cdot G2$

The final block in the overall flowchart for system model PRx, "Set initial V_{rect_target} and Pr_max based on $G1 \cdot G2$ ", is shown as follows:

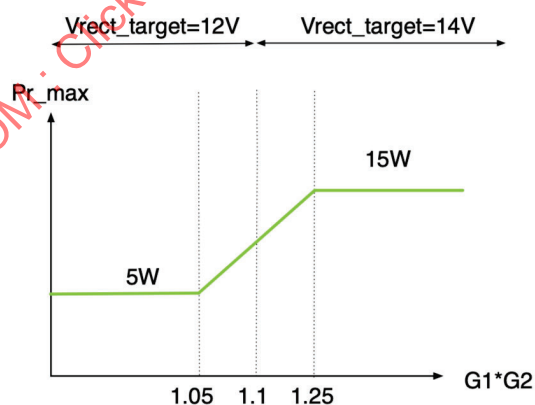
Figure 5.9.2.3.3: 53 Set initial Vrect_target and Pr_max based on G1*G2 .



Any Vrect target value set in this flowchart serves as the initial value in the system model. During power transfer, the system model updates Vrect target according to Figure 5.2.1.5: 35 .

Using the formula in the flowchart, Pr_max exhibits a linear relationship with gain in the normal operating range:

Figure 5.9.2.3.3: 54 Pr_max vs G1*G2 .



4.9.2.3.4 Low-k Mode

When the measured gain is low, it indicates that the coupling between PTx and PRx is low, and the system model PRx sets the "Low-K power profile" field in the SRQ/pcp packet (MPP Protocol spec 8.1.11) to inform PTx.

The system-model PRx sets the low-k field when $G1 \cdot G2 < 1.05$, i.e. when Pr_max is 5W in Figure 5.9.2.3.3: 54 . This would occur when the PRx is outside of the 2x2 cylinder and with a steep load line. In this case, a load release event can lead to OVP and consequently a disconnect. To prevent this, when the system-model PTx receives an SRQ/pcp packet with the low-k field set, it reduces the maximum allowed Vin from 20V to 18V (see Table 5.3-17). This is to avoid over-voltage caused by the steep output impedance (See § 5.8.1.1 Slope of the output Impedance) at the top range of Vin when the coupling is low.

4.9.3 PTx Specifications

Section	Specification	Description
5.9.3.0.1	PTx Pr_max Spec 1	PTx shall send a VINV packet reply when it receives a GET INV packet from the receiver (§ 5.9.4.1).
5.9.3.0.2	PTx Pr_max Spec 2	Upon receiving a GET INV request, the PTx shall hold its Vinv level for 20s or until a non-zero XCEV, whichever comes first.

4.9.4 PTx Specification Notes

Section	Specification	Description
5.9.4.1	Equivalent Vinv	Equivalent Vinv is defined as a value equal or proportional to the first harmonic of PTx's inverter voltage output. For example, the system model PTx follows the full-bridge design in Figure 5.3.1: 36 , and the following is a valid definition of Vinv: $V_{inv} = V_{in} \sin \frac{\pi - \theta}{2} \approx V_{in} \left(1 - \frac{1}{2} \left(\frac{\pi}{2} \right)^2 x^2 + \frac{1}{24} \left(\frac{\pi}{2} \right)^2 x^4 \right), \quad x \triangleq \frac{\theta}{\pi}$ where the definition of phase θ follows the definition in § 5.10.2.1.1 System-level block diagrams .

4.10 Power Transfer Control

4.10.1 Intro and Background (Informative)

The purpose of this section is to describe the MPP end-to-end (E2E) closed-loop control, including: principle, algorithms, control flows, state machines, system modeling and guidance on the design of controllers.

MPP PTx/PRx system generally should comprise of the following hardware components:

- (PTx) Wall adapter facing DC/DC converter
- (PTx) DC/AC Inverter
- (PTx and PRx) Coil Module
- (PRx) AC/DC Rectifier
- (PRx) Battery charger

and the following control components:

- (PRx) Charger Ilim loop
- (PRx) Vrect target loop and XCE generation
- (PTx) XCE to inverter drive (Vin and phase) conversion

A generic system-level hardware and control block diagram is shown in § 5.10.2.1.1 System-level block diagrams .

4.10.2 System Model

4.10.2.1 Background and Assumptions

The following sections depict the design of end-to-end power delivery control system between PTx and PRx in the system model. Designers of custom MPP PTx and PRx can use the following design as a reference.

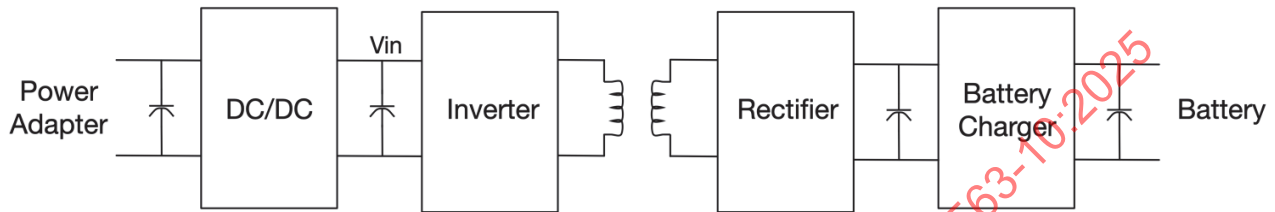
In the system model below, we make the following assumptions to the underlying hardware:

- PTx uses a full-bridge inverter, such that we can adjust inverter input voltage (V_{in}) and phase (θ) to increase or decrease drive to PTx coils.
- PRx can limit the current going into the load (battery and systems) by setting I_{lim} .

Designers should make their end-to-end control systems design is customized to their hardware needs, as long as the design meets the requirement spec set forth in § 5.10.3 End-to-End Control Specifications .

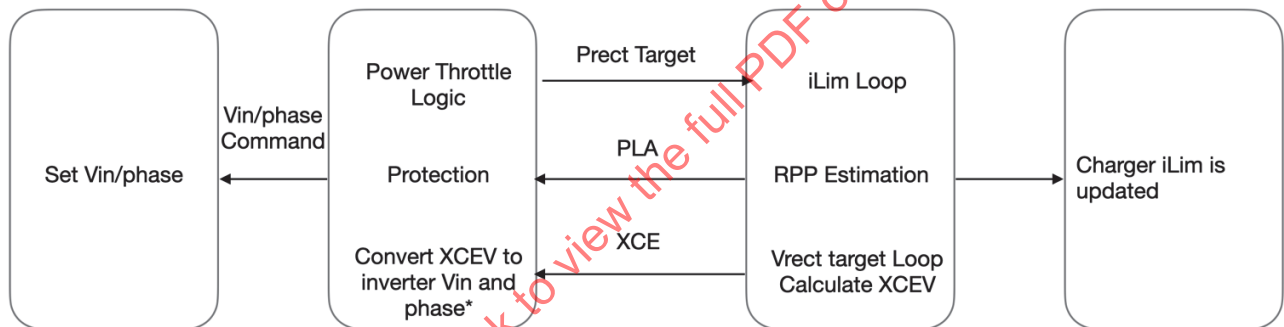
4.10.2.1.1 System-level block diagrams

High-level hardware block diagram:



In the system model, we use a full-bridge inverter.

End-to-end control systems block diagram:



* Please see § 2.3.3 Symbols for the definition of inverter V_{in} and phase (θ)

4.10.2.1.2 Design considerations

System model's E2E closed-loop control pursues the following objectives:

- Fast convergence to steady states
- Fast ramp up to target power
- High resilience to physical motion and system load fluctuations
- High efficiency to reduce the thermal significant loss (TSL) and improve charging time
- Wide range of power controllability to accommodate wide system load and Tx-Rx couplings
- No power adapter brownout during power ramping up or physical motion

However, the E2E control is complicated by several system interactions, including:

- Slow in-band comm
- Load fluctuations
- Nonlinear gain of inductive DC-DC system (load and coupling dependences)
- Limited power sink capacity with high state of charge of battery
- Physical motion of Rx and Tx
- Tx voltage/power controllability
- Limited power adapters (low power rating or loose USB-C connection)

- System thermal constraints

4.10.2.2 Vrect_target Loop (PRx+PTx)

The objective of the Vrect_target loop is to increase or decrease the power from PTx with a fastest possible way while still maintaining stable operation. The PRx requests increasing or decreasing the PTx Vboost voltage or inverter phase by sending the XCE packet to the PTx. Based on the received XCE value (XCEV), PTx will adjust the Vin and phase to increase or decrease inverter drive.

XCEV is calculated as proportional to the difference between target Vrect (Vrect_target) and measured Vrect.

Specifically, in the system model, Vrect is sampled by a calibrated ADC every 10ms, outside of comms (ASK and FSK), and averaged between two consecutive XCE packets. XCEV can be calculated as:

$$XCEV = \left\lfloor 128 \times \frac{V_{RECT_TARGET} - V_{RECT}}{V_{RECT_TARGET}} + \frac{1}{2} \right\rfloor$$

where $\lfloor x \rfloor$ is the floor function that takes the largest integer no larger than the floating-point value x .

4.10.2.2.1 PTx Control

With inverter frequency fixed, PTx controls the power by adjusting the voltage applied to the inductive ac link based on the XCE packets from PRx. This can be achieved by either

- (Vin control mode) adjusting the inverter input voltage Vin to the inverter between VIN_MIN and VIN_MAX, or
- (phase control mode) adjusting the inverter phase θ (see § 5.3.1.1 Definition of inverter phase θ) between PHASE_MIN and PHASE_MAX.

In the system model, both legs of the full-bridge inverter always maintain 50% duty cycle.

Usually, VIN_MIN and VIN_MAX are determined by the dc/dc converter and the system requirement, and PHASE_MIN is limited by ZVS constraints and non-monotonic behavior of the inverter.

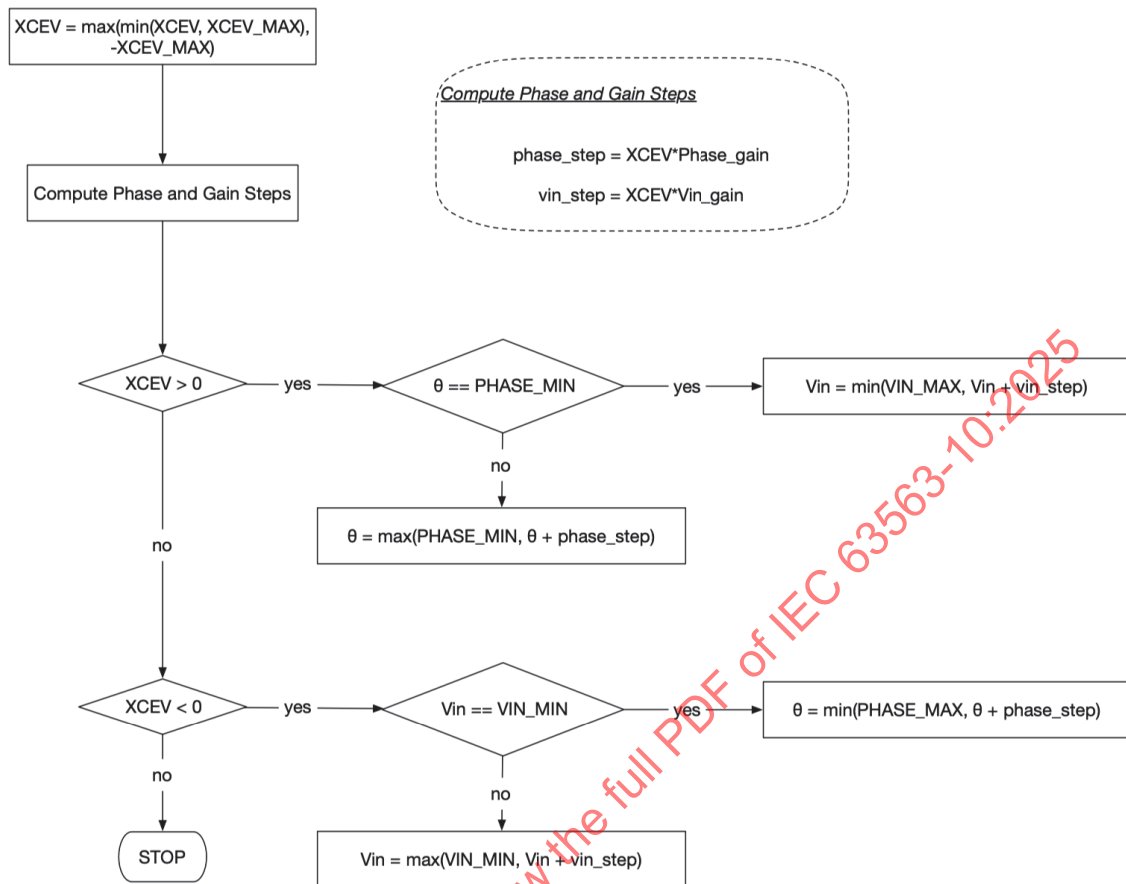
The system model *only* changes inverter phase θ to be above PHASE_MIN when it's *not* possible to reach the desirable drive by adjusting Vin only. Therefore,

- in phase shift control mode and when inverter phase θ is reaching PHASE_MIN (i.e., requesting more power), the system will fix the phase to be PHASE_MIN and switch to Vin control mode; and
- in Vin control mode and when Vin is reaching VIN_MIN or less (i.e., requesting less power), Vin will be fixed at VIN_MIN and switch to phase control loop.

The transition diagram is summarized in Figure 5.10.2.2.1: 55 .

From control systems perspective, the system model employs a simple proportional controller, where we adjust Vin or phase proportionally to Vrect control error received. Vin or phase shall be adjusted in hardware after the ASK packet was decoded and passed parity and checksum check. It should leave enough time for Vrect to stabilize and reach steady state before the next XCE packet is received. See Chapter 4.2 in MPP Communications Protocol for the exact timing requirement.

Figure 5.10.2.2.1: 55 Tx Voltage Control Flow Chart .



In the system model, the parameters used in the flow charts are:

- [VIN_MIN, VIN_MAX] = [11 V, 19 V]
- [PHASE_MIN, PHASE_MAX] = [0°, 50°]
- Phase_gain = -0.16°
- Vin_gain = 16mV
- XCEV_MAX = 64

A few notes on Figure 5.10.2.2.1: 55 :

- Please note that the inverter phase θ and V_{in} affect inverter power in opposite directions:
 - as the inverter phase θ increases, the inverter output decreases
 - as V_{in} increases, the inverter output increases
- If the inverter phase θ reaches PHASE_MIN and V_{in} reaches VIN_MAX, the "Status" field in the RCS packet should be set to 3, indicating that we've reached the maximum supported voltage (MPP Protocol Spec 7.2.2)
- In the system model, when the inverter phase θ reaches PHASE_MIN, the remaining balance of CEP value is discarded and does not apply to a new vin_step remainder; and vice versa when V_{in} reaches VIN_MIN. So around θ/V_{in} adjustment boundary, an XCE packet may appear not to be fully acted upon. A practical MPP transmitter may choose to apply the remainder to fix this, but for the system model we decided to take the simpler approach.
- Since both θ and V_{in} control has fixed resolutions (See Table 5.3.1.3: 18), the calculated V_{in} or θ is truncated to a multiple of its respective resolutions. Any error left will be added to the next calculation. For example, if we receive XCEV=1 and we are in the V_{in} adjustment regime, a single step (16mV) is smaller than V_{in} resolution (30mV); so

we will need to accumulate two XCEV=1 packets to adjust V_{in} by 30mV, and the 2mV remainder to be applied to the next calculation.

It can be seen from Figure 5.10.2.2.1: 55 that V_{in} is adjusted up or down by vin_step , or phase is adjusted up or down by $phase_step$ from the current level. Thus, the V_{in} and phase values are the accumulation of all vin_step and $phase_step$ adjustments. Hence, the voltage regulation control loop is the integral of the ($V_{rect_target} - V_{rect}$) error. The update rate of the voltage regulation loop is slow compared to the load dynamics and therefore stability of this loop is guaranteed if the XCEV correction steps are small enough so that the V_{rect} target is not overshoot at any coupling position or regulation operating point (specifically, there will be no oscillation in the closed-loop response if the open-loop gain is less ≤ 1).

4.10.2.3 Ilim Loop (PRx)

The Ilim loop is designed to maximize the power transfer of the link in whatever physical state it exists. Within this loop, the § 5.10.2.2.1 PTx Control and physical coupling are assumed to vary slowly compared to the update rate of the loop. However, the state of the loop will vary with time, and there is significant uncertainty in the transfer function of the system at any moment. These challenges suggest the use of an algorithm with limited assumptions and high resilience to noise, drift, and transfer function changes.

4.10.2.3.1 Load Current Control

The system model PRx controls the power ramp up by setting a current input ceiling to the load which is allowed to increase gradually. Typically for a phone, the "load" here means a battery charger or a power management system that supplies power to the battery and rest of the phone hardware system.

Let I_{sns_max} denote the maximum current sourced by the rectifier over a measurement interval (for instance, maximum of 10 measurements made over 100ms). At the end of the measurement interval, PRx sets

$$I_{LIM} = I_{SNS_MAX} + \Delta I$$

where ΔI is small, but larger than the maximum buck converter regulation error plus at least 1 LSB (see the system-model PRx block diagram in § 5.2 Power Receiver Functional Block-Diagram). Specifically, in the system model, $\Delta I = 40mA$, so the buck converter can increase the current load by up to 40mA and the maximum power ramp rate is controlled to $40mA * V_{RECT}$ per measurement interval. The measurement interval is much slower than the charger settling time. The current ceiling, I_{LIM} , is limited also by the maximum power negotiated between PTx and PRx.

4.10.2.3.2 Ilim Freeze and Anti-Crash Mechanism

In addition to the regular § 5.10.2.3.1 Load Current Control , the system model employs two additional mechanisms that limit Ilim increase/decrease to increase V_{rect} stability:

1. Ilim freeze: if Ilim value is increased too aggressively such that V_{rect} drops much below V_{rect} target, we will "freeze" Ilim such that it cannot increase any more, until V_{rect} rises back through the XCE Loop.
2. Anti-crash: in rare cases, if V_{rect} continues to drop over the said limit in 1 (i.e., V_{rect} crashes), then we will force Ilim to ramp down as an attempt to bring back V_{rect} . For example, the power ramp-down can be governed by the following formula:

$$I_{LIM} = I_{SNS_MAX} + \Delta I \cdot \frac{V_{RECT} - (V_{RECT_TARGET} - 0.8V)}{0.5V}$$

However, to avoid large reductions in power and swings in V_{rect} , we limit this Ilim reduction to 100mA.

Figure 5.10.2.3.3: 56 provides a view of the Ilim control, as well as all the thresholds we use to trigger Ilim freeze and anti-crash protection.

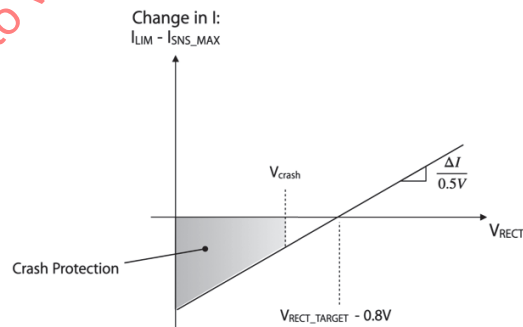
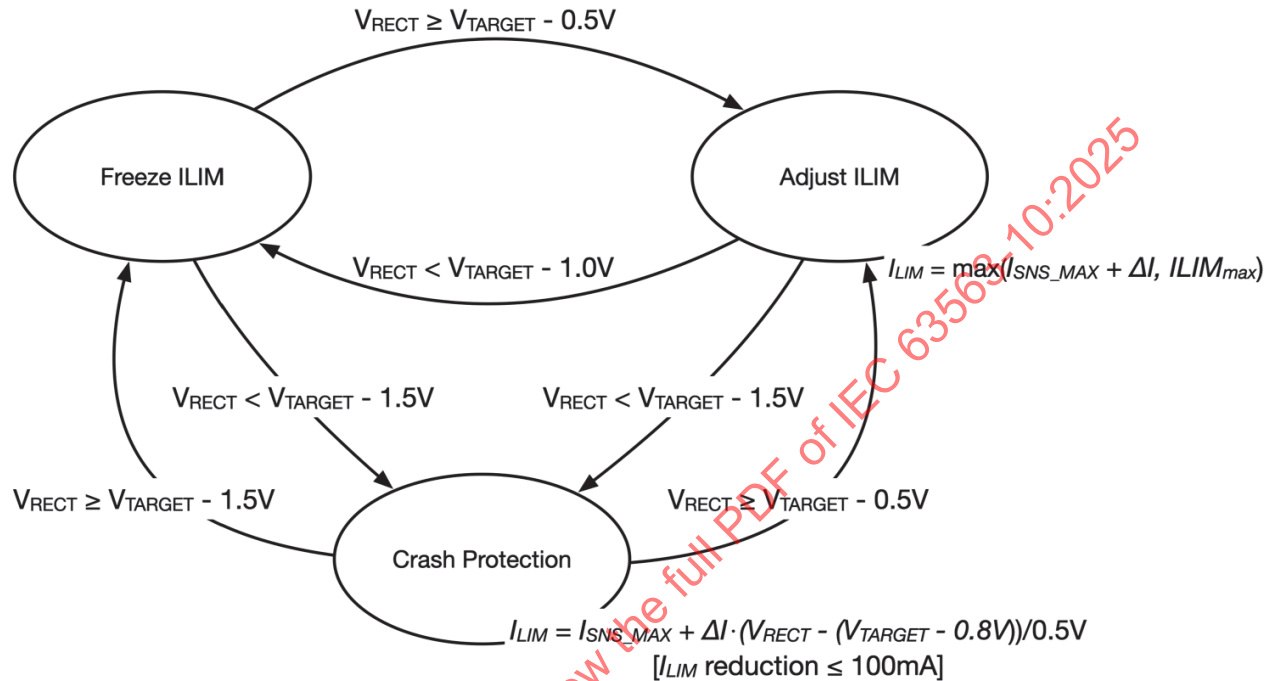
Additionally, while PRx is in Ilim freeze or anti-crash mode, as an attempt to speed up V_{rect} recovery to V_{rect_target} , we also increase the frequency of XCE packets. Normally, XCE packets are sent every 560ms in the system model; in Ilim freeze or anti-crash mode, we decrease the XCE packets interval to 80ms.

Ilim freeze and anti-crash mechanism also provide a practical implementation to meet § 5.10.3.4.5 .

4.10.2.3.3 Loop Update Interval

Normally, Ilim has an update interval of $ILIM_TIME_MIN = 100ms$. Ilim loop does not perform any adjustment while FSK or ASK is active because V_{RECT} and $ISNS$ are perturbed by frequency change or load change.

Figure 5.10.2.3.3: 56 Ilim control diagram .



Notes on Figure 5.10.2.3.3: 56 :

- Each time when V_{rect} target changes (according to Figure 5.2.1.5: 35), "crash protection" state is disabled for 10s. This is to prevent false triggers of crash protection during transitions of V_{rect} target.
- There is no hysteresis between the "Freeze ILIM" and "Crash Protection" states. This is intentional, because:
 - The crash protection formula has a "gained response" where the reduction of Ilim decreases as V_{rect} approaches back to V_{rect} target. It already helps to mitigate oscillation, as what hysteresis would do. It's unlike the other situation in the diagram where we have hysteresis when Ilim increase is constantly ΔI .

- We'd like to limit the region where power decreases, and if we lower power until $V_{rect} \geq V_{target} - 1.5V$, there is a risk of too large power reduction.

4.10.2.4 Power throttling

The power throttling is the most outside layer in the control hierarchy where both Tx and Rx are working together to identify if the power level is sustainable. The Tx available power level is limited by the USB adapter, FOD losses, system thermals and electrical rating of the Tx hardware. Tx will estimate the available power based on various limits and send it to Rx by in-band communication. After receiving the available power from Tx, the Rx will set a target power based on the sinking capability is limited by Rx system thermals, electrical rating of Rx hardware.

There are various sources which may request power throttling:

- Dc/dc converter OCP
- Foreign object P_FO over limit
- Thermal (PTx/PRx) protection

Each individual power throttling source will have its own P_{rect_target} output based on the specific algorithm. Tx will renegotiate single P_{rect_target} with the minimum P_{rect_target} from all sources. To reduce the comms traffic, Tx shall only renegotiate power with Rx when the P_{rect_target} delta is greater than $\pm 100mW$ between current and previous target values.

If any of the above protections are triggered, the "Status" field in the RCS packet should be set to 2 (MPP Protocol Spec 7.2.2)

4.10.3 End-to-End Control Specifications

4.10.3.1 Background

End-to-end control loop stability and predictability is important for an MPP PTx and PRx to inter-operate correctly and reach equilibrium for stable power delivery. We achieve this by requiring PTx and PRx to follow § 5.10.3.2 PTx Specifications and § 5.10.3.4 PRx Specifications respectively.

4.10.3.2 PTx Specifications

Below are the MPP end-to-end control specifications for PTx:

When testing a custom-designed PTx for MPP compliance, it's mated with a Test PRx (TPR) that follows the PRx implementation in the informative session (§ 5.10.2 System Model)

Section	Specification	Description
5.10.3.2.1	PTx E2E Spec 1	Upon receipt of $XCEV > 0$, PTx shall increase PTx drive level (See note § 5.10.3.3.1 for the definition of drive level), unless a protection is triggered.
5.10.3.2.2	PTx E2E Spec 2	Upon receipt of $XCEV < 0$, PTx shall decrease PTx drive level.
5.10.3.2.3	PTx E2E Spec 3	Upon receipt of $XCEV = 0$, PTx shall not increase or decrease PTx drive level during normal operation, unless a protection is engaged.
5.10.3.2.4	PTx E2E Spec 4	For a constant-current TPR load, with any $P_{rect} \leq 15W$, PTx shall drive V_{rect} to converge to its target without overshoot or undershoot, defined in § 5.10.3.3.2 . See note § 5.10.3.3.1 , § 5.10.3.3.2 , § 5.10.3.3.3 , § 5.10.3.3.4 , 5.
5.10.3.2.5	PTx E2E Spec 5	For a constant-current TPR load, with any $P_{rect} \leq 15W$, PTx shall drive V_{rect} to converge to its target within 30 XCE packets received from PRx. See note § 5.10.3.3.1 , § 5.10.3.3.2 , § 5.10.3.3.3 , § 5.10.3.3.4 .
5.10.3.2.6	PTx E2E Spec 6	The slope of the output impedance shall meet the following requirement: with a constant PTx drive level, during any Prx load release from 7.5W, there will be no OVP triggered on Prx. See § 5.8.1.1 Slope of the output Impedance for the definition of output impedance.

Section	Specification	Description
		See § 5.11.1.2 Receiver overvoltage protection for the OVP implementation by the system model PRx.
5.10.3.2.7	PTx E2E Spec 7	The PTx shall have a control resolution such that the Vrect on the TPR has a maximum step size of 0.25V within $\pm 0.5V$ window of 15V, with a load current of 50mA at position (0,0).

4.10.3.3 PTx Specification Notes

Section	Specification	Description																											
5.10.3.3.1	PTx E2E Note 1	<p>In compliance test corresponding to PTx specifications § 5.10.3.2.1 , § 5.10.3.2.2 , § 5.10.3.2.3 , § 5.10.3.2.4 and § 5.10.3.2.5 , we create the initial state of the test by:</p> <ol style="list-style-type: none"> 1) having the PTx converged, as defined in note § 5.10.3.3.2 ; 2) applying a step change ΔI_{load} in the PRx load current from converged steady state, so that Vrect diverges from Vrect_target. <p>After the initial state, TPR will be in a constant-current mode with the new Iload. It will:</p> <ul style="list-style-type: none"> • send XCE packets to PTx as specified in § 5.10.3.2 Vrect_target Loop (PRx+PTx) and allow PTx to change its drive for Vrect to re-converge to Vrect_target; • monitor its Vrect as per specified in PTx specifications § 5.10.3.2.1 , § 5.10.3.2.2 , § 5.10.3.2.3 , § 5.10.3.2.4 and § 5.10.3.2.5 ; and • monitor its Prect after PTx has converged, as defined in note § 5.10.3.3.2 . <p>Below is a table of how Iload changes to create the initial condition, and what's the expected range of Prect after PTx has converged:</p> <table border="1"> <thead> <tr> <th>(x,z)</th><th>initial condition (Vrect_target,Iload)</th><th>New (Vrect_target,Iload)</th></tr> </thead> <tbody> <tr> <td>(0,0)</td><td>(12, 0.050)</td><td>(12, 0.625)</td></tr> <tr> <td></td><td>(12, 0.625)</td><td>(12, 0.050)</td></tr> <tr> <td></td><td>(14, 0.500)</td><td>(14, 1.071)</td></tr> <tr> <td></td><td>(14, 1.071)</td><td>(14, 0.500)</td></tr> <tr> <td>(2,2)</td><td>(12, 0.050)</td><td>(12, 0.500)</td></tr> <tr> <td></td><td>(12, 0.625)</td><td>(12, 0.400)</td></tr> <tr> <td></td><td>(14, 0.500)</td><td>(14, 0.700)</td></tr> <tr> <td></td><td>(14, 1.071)</td><td>(14, 0.900)</td></tr> </tbody> </table>	(x,z)	initial condition (Vrect_target,Iload)	New (Vrect_target,Iload)	(0,0)	(12, 0.050)	(12, 0.625)		(12, 0.625)	(12, 0.050)		(14, 0.500)	(14, 1.071)		(14, 1.071)	(14, 0.500)	(2,2)	(12, 0.050)	(12, 0.500)		(12, 0.625)	(12, 0.400)		(14, 0.500)	(14, 0.700)		(14, 1.071)	(14, 0.900)
(x,z)	initial condition (Vrect_target,Iload)	New (Vrect_target,Iload)																											
(0,0)	(12, 0.050)	(12, 0.625)																											
	(12, 0.625)	(12, 0.050)																											
	(14, 0.500)	(14, 1.071)																											
	(14, 1.071)	(14, 0.500)																											
(2,2)	(12, 0.050)	(12, 0.500)																											
	(12, 0.625)	(12, 0.400)																											
	(14, 0.500)	(14, 0.700)																											
	(14, 1.071)	(14, 0.900)																											
5.10.3.3.2	PTx E2E Note 2	<p>Regulation to Vrect target is indicated by $XCEV \leq 3$ for 5 consecutive XCE packets.</p> <p>An overshoot or undershoot occurs if, after the first instance where Vrect is regulated (note § 5.10.3.3.2), Vrect becomes unregulated again.</p>																											
5.10.3.3.3	PTx E2E Note 3	All PTx requirements in this section shall hold over the 2x2 power delivery cylinder.																											
5.10.3.3.4	PTx E2E Note 4	<p>Increasing or decreasing PTx drive level refers to mechanisms to increase or decrease the magnetic field that the PTx generates. For a typical PTx design as demonstrated in figure § 5.10.2.1.1 System-level block diagrams , increasing PTx drive means increasing Vin or decreasing phase, and decreasing PTx drive means decreasing Vin or increasing phase. PTx drive level is positively related to § 5.9.4.1 .</p> <p>A TPR detects PTx drive increase (spec § 5.10.3.2.1) by measuring its Vrect and check if the new Vrect is larger than Vrect-Vhys, where Vhys is an allowed hysteresis. Similarly, A TPR detects PTx drive decrease (spec § 5.10.3.2.2) if the new Vrect is smaller than Vrect+Vhys; a PTR detects that</p>																											

Section	Specification	Description
		PTx drive remains the same (spec § 5.10.3.2.3) if the new Vrect falls within the range bounded by $V_{rect} \pm V_{hys}$. V_{hys} is defined as 0.5V in MPP compliance tests for PTx.

4.10.3.4 PRx Specifications

Below are the MPP end-to-end control specifications for PRx:

When testing a custom-designed PRx for MPP compliance, it's mated with a Test PTx (TPT) that follows the system model (§ 5.10.2 System Model)

Section	Specification	Description
5.10.3.4.1	PRx E2E Spec 1	When mated with a TPT, PRx's power transfer control shall converge to a set point, without overshoot or undershoot. See note § 5.10.3.6.2 for the test condition and definition of over/undershoot.
5.10.3.4.2	PRx E2E Spec 2	When mated with a TPT, PRx shall reach regulation in less than 30s after sending the signal strength packet. See note § 5.10.3.6.2 for the test condition and definition of reaching regulation.
5.10.3.4.3	PRx E2E Spec 3	PRx shall limit its load current increase to 40mA/100ms.
5.10.3.4.4	PRx E2E Spec 4	PRx's Prect shall not be higher than Prect target by $\max(50\text{mW}, 0.1 * P_{rect_target})$ sustained for longer than 100 ms.
5.10.3.4.5	PRx E2E Spec 5	If PTx drops its equivalent V_{in} by at least 0.2V (see § 5.9.4.1) asynchronously (see § 5.10.3.6.4), PRx shall adapt its power draw such that PTx observes inverter power decrease proportionally within 200 ms. See § 5.10.3.6.3 for the definition of proportionality. See § 5.10.2.3 Ilim Loop (PRx) for the system model's implementation to meet this spec.

4.10.3.5 PRx Recommendations

Section	Specification	Description
5.10.3.5.1	PRx load release	If PRx releases its load too quickly, then there could be a spike increase of Vrect voltage, and may trigger OVP (over-voltage protection). Therefore, PRx should limit how quickly its load can decrease. Here is a recommended table: - when Prect is larger than 7W, maximum ΔP_{rect} should be limited by the following rule: <ul style="list-style-type: none"> • $7 < P_{rect} \leq 8$: $\Delta P_{rect} < 3.2$ • $8 < P_{rect} \leq 9$: $\Delta P_{rect} < 3$ • $9 < P_{rect} \leq 10$: $\Delta P_{rect} < 2.7$ • $10 < P_{rect} \leq 11$: $\Delta P_{rect} < 2.5$ • $11 < P_{rect} \leq 12$: $\Delta P_{rect} < 2.3$ • $12 < P_{rect} \leq 13$: $\Delta P_{rect} < 2.1$ • $13 < P_{rect} \leq 14$: $\Delta P_{rect} < 1.9$ • $14 < P_{rect} \leq 15$: $\Delta P_{rect} < 1.6$ - when Prect is less than or equal to 7W, PRx should be allowed to release the load all the way to the minimal current level (50mA for the system model, see § 5.9.2.2 PRx ballast current) in a single step
5.10.3.5.2	Prect Vrect Target	PRx should regulate to steady Vrect target(s). Vrect target should be constant for a given Prect target.
5.10.3.5.3	XCEV proportionality	PRx should implement XCEV proportional to the Vrect target error ($V_{rect_target} - V_{rect}$)

4.10.3.6 PRx Specification Notes

Section	Specification	Description
5.10.3.6.1	PRx E2E Note 1	All PRx requirements in this section shall hold over the 2x2 power delivery cylinder.
5.10.3.6.2	PRx E2E Note 2	Regulation to Vrect target is indicated by $ XCEV \leq 3$ for 5 consecutive XCE packets. An overshoot or undershoot is detected if Vrect target becomes unregulated ($ XCEV > 3$) again immediately after 5 XCE packets with $ XCEV \leq 3$.
5.10.3.6.3	PRx E2E Note 3	The definition of proportionality goes as follows: If PTx voltage drops from V_1 to V_2 and the measured PTx inverter power goes from P_1 to P_2 , then we require that $P_2 \leq P_1 V_2 / V_1$, within measurement tolerance.
5.10.3.6.4	PRx E2E Note 4	PTx's asynchronous adjustment of equivalent Vin is defined as adjustments that do not correspond to a negative XCE packet. This may happen if, for example, PTx enters a protection state the requires urgent power reduction.

4.11 Mitigation of Side Effects of Cd at MPP Frequency

4.11.1 System Model

Cd, the 1MHz parallel capacitor required by Qi, resonates close to the 3rd harmonic of 360kHz. This resonance causes several challenges:

- Potentially non-monotonic Vrect/phase response and steep output impedance at light load;
- Susceptibility of receiver over voltage;
- Breaking ZVS, which may cause excessive loss and emission problems.

We'll go through how the system model deals with these challenges in the following subsections.

4.11.1.1.1 Non-monotonic Vrect/phase response and output impedance at light load

Figure 5.11.1.1.1: 57 shows that at light load, Vrect isn't necessarily monotonic with inverter phase (See § 2.3.3 Symbols for the definition of inverter phase θ). For monotonic response, maximum inverter phase is limited to 50 degrees.

Having a small phase limit also helps in limiting the slope of the output impedance, see Figure 5.11.1.1.1: 58 . Having a shallow output impedance slope helps to improve control stability and reduce the risk of over-voltage (see § 5.8.1.1 Slope of the output Impedance).

Figure 5.11.1.1.1: 57 Vrect vs inverter phase at light load .

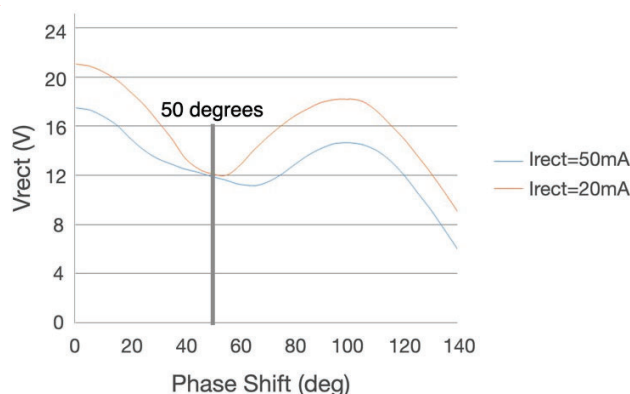
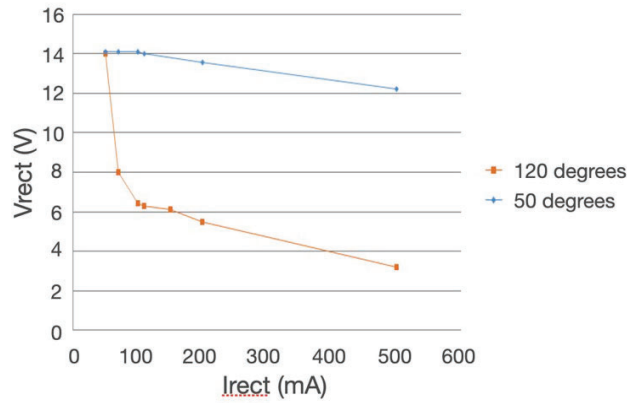


Figure 5.11.1.1.1: 58 Output impedance with 50 and 120 degrees inverter phase .



4.11.1.1.2 Over-voltage mitigation

Cd increases the system gain (V_{rect} / V_{in}) especially at 1MHz (See Figure 5.11.1.1.2: 59), making it easier to trigger over-voltage protection at the receiver side.

To mitigate this risk, in the system model,

- max load step is limited in the PRx,
- load current clamp and rectifier diode mode are added, and
- V_{rect} target voltage is kept low
- low-k mode is introduced (§ 5.9.2.3.4 Low-k Mode)

In Figure 5.11.1.1.2: 60 , these are referred to as "mitigations".

Figure 5.11.1.1.2: 59 Gain (V_{rect}/V_{in}) with and without Cd .

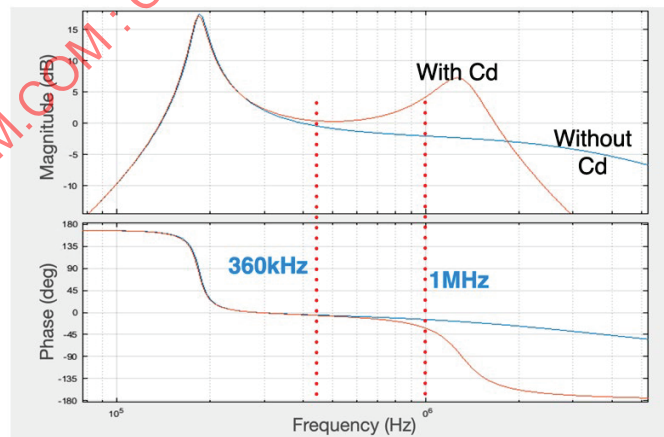
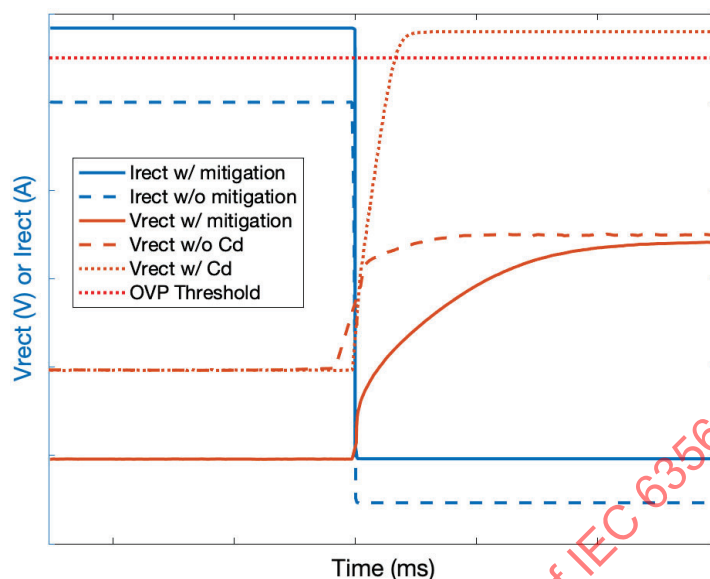


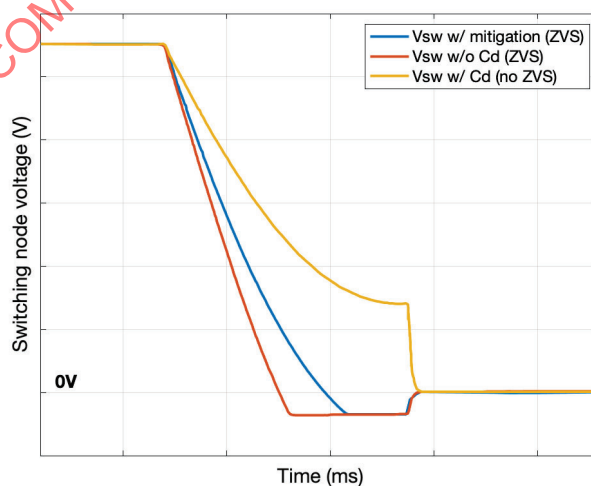
Figure 5.11.1.1.2: 60 Load release from 7W to 0W, with and without Cd, and with mitigations implemented in the system model .



4.11.1.1.3 Hard switching mitigation

In the system model, ZVS is generally maintained to reduce loss and limit emissions. Having Cd increases the risk of losing ZVS, and we mitigate this risk by making sure that the input impedance viewed from the PTx side is always inductive (impedance phase is always larger than 20 degrees). This is done via selecting the transmitter resonant cap so that the resonant frequency is reduced. See Figure 5.11.1.1.3: 61 .

Figure 5.11.1.1.3: 61 ZVS state with and without Cd, and with mitigations implemented in the system model .



4.11.1.2 Receiver overvoltage protection

In the system model, if rectified voltage exceeds 21V, PRx protects its circuit by connecting AC1 and AC2 nodes to GND until Vrect is below 15V.

To make sure that PRx's over-voltage protection works without damaging PRx circuit, PTx needs to follow § 5.11.2.1 .

4.11.2 Specifications

Section	Specification	Description
5.11.2.1	PTx OCP Spec 1	PTx shall implement over-current protection, such that when TPR connects AC1 and AC2 nodes together, the sustained peak current through the PRx coil is less than 6.7A, until XCE times out.

4.12 Cloak

Cloaking lets a wireless charging system to pause active power transfer while still maintaining a Tx-Rx link such that power transfer can be resumed any time without going through the entire start up flow and power negotiation stages.

Power pause / cloak may be used in scenarios such as

1. Wireless power system may enter power pause (cloak) to allow power receiver to perform an NFC scan
2. Wireless power system may enter cloak for thermal management
3. Wireless power system may enter cloak for environmental reasons such as power savings at end of charge

4.13 Common-mode Noise

Excessive common-mode noise generated by PTx can interfere with the proper operation of the display and touch system on PRx. PTx manufacturers should perform due diligence in their design process to avoid this.

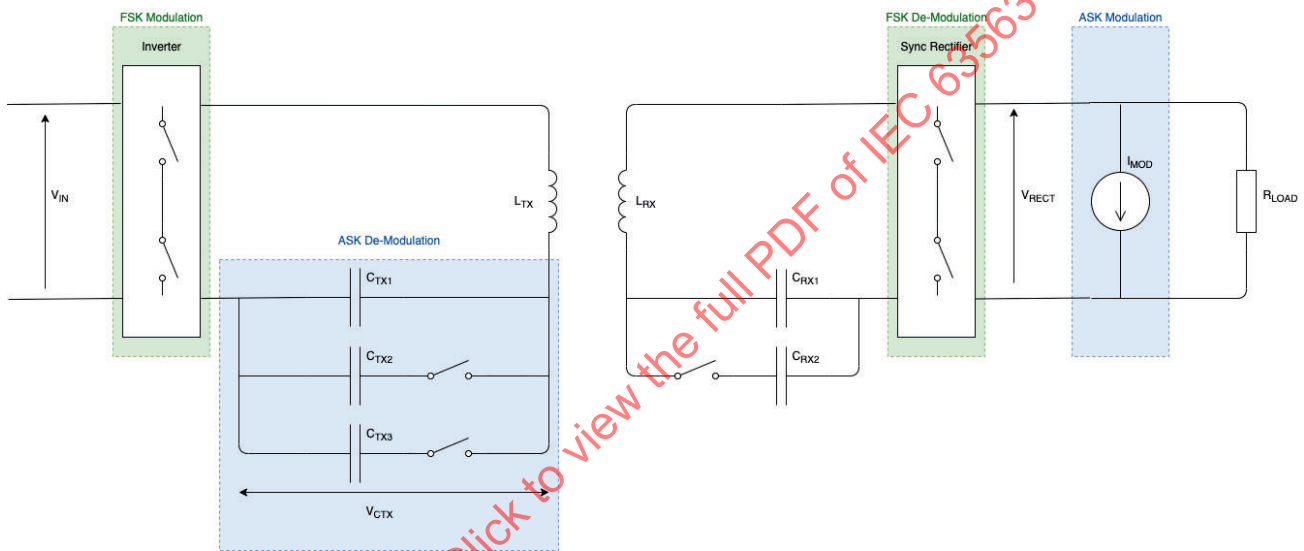
5 Communications Physical Layer

5.1 Introduction

This section describes the physical communications layer that is implemented in MPP and the corresponding specifications for an MPP PTx and PRx.

In MPP mode, the PTx communicates to the PRx by modulating the inverter frequency and therefore the power signal frequency. This can be demodulated on the PRx as part of the synchronous rectification process. The PRx uses backscatter modulation to communicate back to the PTx. For this purpose, the PRx modulates the amplitude of the power signal by changing its load. The PTx can demodulate this signal by measuring the voltage across the resonant capacitor (V_{CTX}). A figure of the system model is shown in Figure 6.1: 62 .

Figure 6.1: 62 MPP Comms Physical System Model .



5.2 Frequency Shift Keying (PTx to PRx)

The MPP system model uses the FSK modulation bit encoding scheme as defined in Section 3.1 of the Qi Communications Physical Layer Specification v2.0 and uses the following modulation parameters:

Parameter	Value	
	MPP (128 kHz digital ping)	MPP (360 kHz ramp up ping and power transfer)
Power Frequency (F_{op})	127.772 kHz	360 kHz
Modulation Frequency (F_{mod})	125.435 kHz	366.412 kHz
Polarity/Depth	Negative/2	Positive/0
Number of Switching Cycles Per Bit (Following CFG packet only)	512	

Number of Switching Cycles Per Bit (following any ASK packet other than CFG)	128
--	-----

5.2.1 System Model

5.2.1.1 FSK Modulator (PTx)

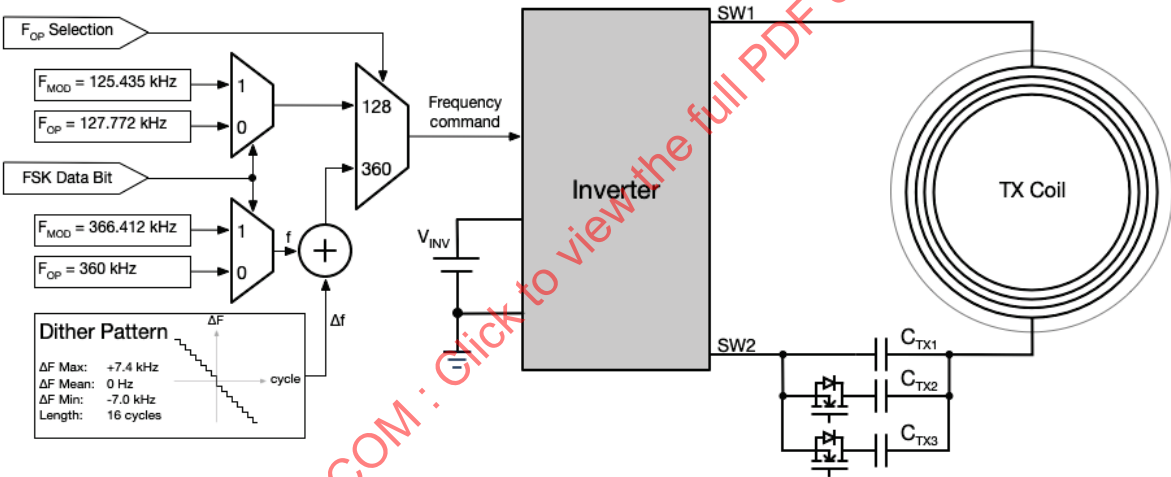
The system model FSK transmitter is presented in Figure 6.2.1.1: 63 . In general, Power Transmitter varies its operating frequency to transmit data to the Power Receiver.

When operating at 128 kHz, the PTx performs FSK modulation by switching between the nominal operating frequency, F_{OP} , of 127.772 kHz and the modulated frequency, F_{MOD} , of 125.435 kHz.

When operating at 360 kHz:

- the PTx performs FSK modulation by switching between the nominal operating frequency, F_{OP} , of 360 kHz and the modulated frequency, F_{MOD} , of 366.412 kHz
- frequency dithering is used, with a repetition length of 16 power frequency cycles and a deviation of -7 kHz to +7 kHz
- the frequency dithering deviation is larger than the FSK modulation depth
- F_{OP} and F_{MOD} values are the averages measured over a period of 16 cycles

Figure 6.2.1.1: 63 System Model for FSK Transmitter .



5.2.1.2 FSK Receiver (PRx)

The system model of a PRx FSK receiver is presented in Figure 6.2.1.2: 64 .

In general, the PRx measures the frequency of the received AC power by measuring the cycle-on-cycle time of the power switching frequency.

The measured cycle times are then processed in the digital domain. The signal chain consists of:

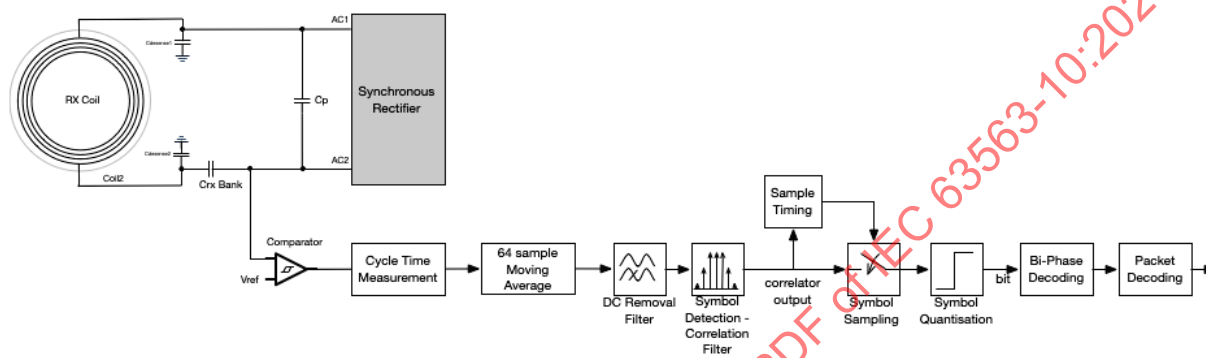
- a moving average filter is used to filter out noise. The length of the filter is 64 cycles, which is an exact multiple of the maximum dither period - 16 cycles. This means the moving average filter will both attenuate random noise and remove dithering signals
- the filtered signal is then passed to a detector / receiver unit

- finally, the receiver takes whichever is available - and correct - first from the Magnitude and Phase detector / receiver units.

The detector / receiver unit:

- may be implemented in hardware, software, or a mixture of the two
- removes DC content from the input signal
- applies symbol detection filters; these detect the specific shape of FSK signal waveforms and remove as much noise as possible
- applies some form of sample timing control such as time counting and peak detection
- samples the incoming data stream to produce a stream of individual encoded bits
- removes the differential bi-phase encoding
- performs packet decoding.

Figure 6.2.1.2: 64 System Model for FSK Receiver .



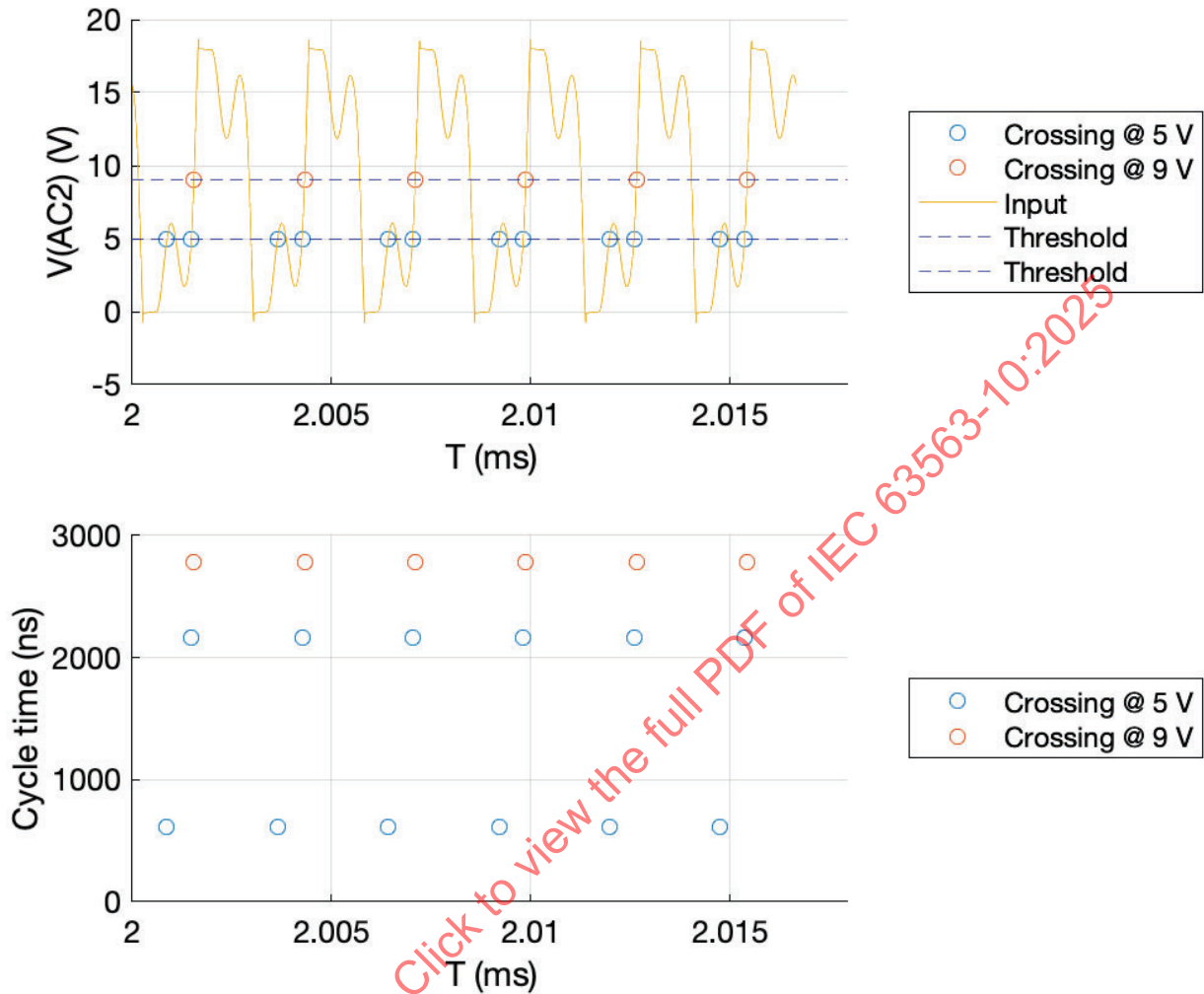
In principle, the FSK detector electronics could be as simple as a comparator which compares the AC1 or AC2 signal to some reference.

However, at light load, the coil current waveforms become distorted by the presence of harmonic content developed by the inverter. In particular, the 3rd harmonic of a 360 kHz power frequency (1.08 MHz) may excite a resonance with the parallel capacitor C_d required to establish a 1 MHz resonance for BPP Analog Ping (refer § 5.2.1 System Model for further information). This can cause oscillations of AC1 and AC2 node voltages, and generate extra crossing events on the comparator output as shown in Figure 6.2.1.2: 65 .

The FSK receiver must include appropriate countermeasures to address this situation, which could include the use of comparator hysteresis, adaptive reference voltage selection or blanking times.

At heavy load, the coil current waveforms are less distorted and extra crossing events tend not to occur.

Figure 6.2.1.2: 65 Sample Waveform: Digital Ping 360 kHz AC2 node voltage .



5.2.2 Frequency Shift Keying Specifications

This section details the frequency modulation specifications for MPP PTx and PRx.

Note: when operating in MPP mode, an MPP Power Transmitter will ignore whatever FSK parameters are requested by the PRx CFG packet and instead use those specified below. Refer to MPP Communications Protocols for further information.

Note: MPP Power Transmitters may employ dithering, as specified in § 5.4 Operating Frequency , which may impact the design of FSK receiver systems.

Section	Specification	Description
6.2.2.1	PTx FSK Spec 1	The MPP Power Transmitter shall transmit FSK signals to the Power Receiver using the same bit encoding method as defined in Section 3.2 of the Qi Communications Physical Layer Specification v2.0.

Section	Specification	Description
6.2.2.2	PTx FSK Spec 2	The MPP Power Transmitter shall transmit FSK signals using a bit period of 128 cycles of the power switching frequency except when transmitted in response to a CFG packet.
6.2.2.3	PTx FSK Spec 3	The MPP Power Transmitter shall transmit FSK responses to the CFG packet using a bit period of 512 cycles of the power switching frequency.
6.2.2.4	PTx FSK Spec 4	The MPP Power Transmitter shall transmit data to the Power Receiver using the same byte encoding scheme as defined in Section 3.3 of the Qi Communications Physical Layer Specification v1.3.1.
6.2.2.5	PTx FSK Spec 5	The MPP Power Transmitter shall transmit Response Patterns as defined in Section 3.5 of the Qi Communications Physical Layer Specification v2.0.
6.2.2.6	PTx FSK Spec 6	In addition to the existing Qi Response Patterns, the MPP Power Transmitter shall transmit the MPP ACK Pattern.
6.2.2.7	PTx FSK Spec 7	The MPP Power Transmitter shall transmit Response Patterns with no preamble.
6.2.2.8	PTx FSK Spec 8	The MPP Power Transmitter shall transmit a preamble consisting of 4 ONE bits before every FSK data packet.
6.2.2.9	PTx FSK Spec 9	The MPP Power Transmitter shall transmit data packets to the Power Receiver using the header field as defined in Section 3.4 of the Qi Communications Physical Layer Specification v2.0.
6.2.2.10	PTx FSK Spec 10	The MPP Power Transmitter shall transmit data packets to the Power Receiver using the message field as defined in Section 3.4 of the Qi Communications Physical Layer Specification v2.0.
6.2.2.11	PTx FSK Spec 11	The MPP Power Transmitter shall transmit data packets to the Power Receiver using the checksum field as defined in Section 3.4 of the Qi Communications Physical Layer Specification v2.0.
6.2.2.12	PTx FSK Spec 12	The MPP Power Transmitter shall transmit adjacent bytes within a data packet such that the stop bit of the preceding byte is immediately followed by the start bit of the following byte.
6.2.2.13	PTx FSK Spec 13	When operating at 128 kHz, the MPP Power Transmitter shall transmit FSK signals using Negative/2 modulation as defined in Section 3.1 of the Qi Communications Physical Layer Specification v2.0.
6.2.2.14	PTx FSK Spec 14	When operating at 360 kHz, the MPP Power Transmitter shall transmit FSK signals using Positive/0 modulation as defined in Section 3.1 of the Qi Communications Physical Layer Specification v2.0.
6.2.2.15	PRx FSK Spec 1	The MPP Power Receiver shall receive and decode FSK transmissions from the Power Transmitter.

5.3 Amplitude Shift Keying (PRx to PTx)

5.3.1 Modulation Scheme

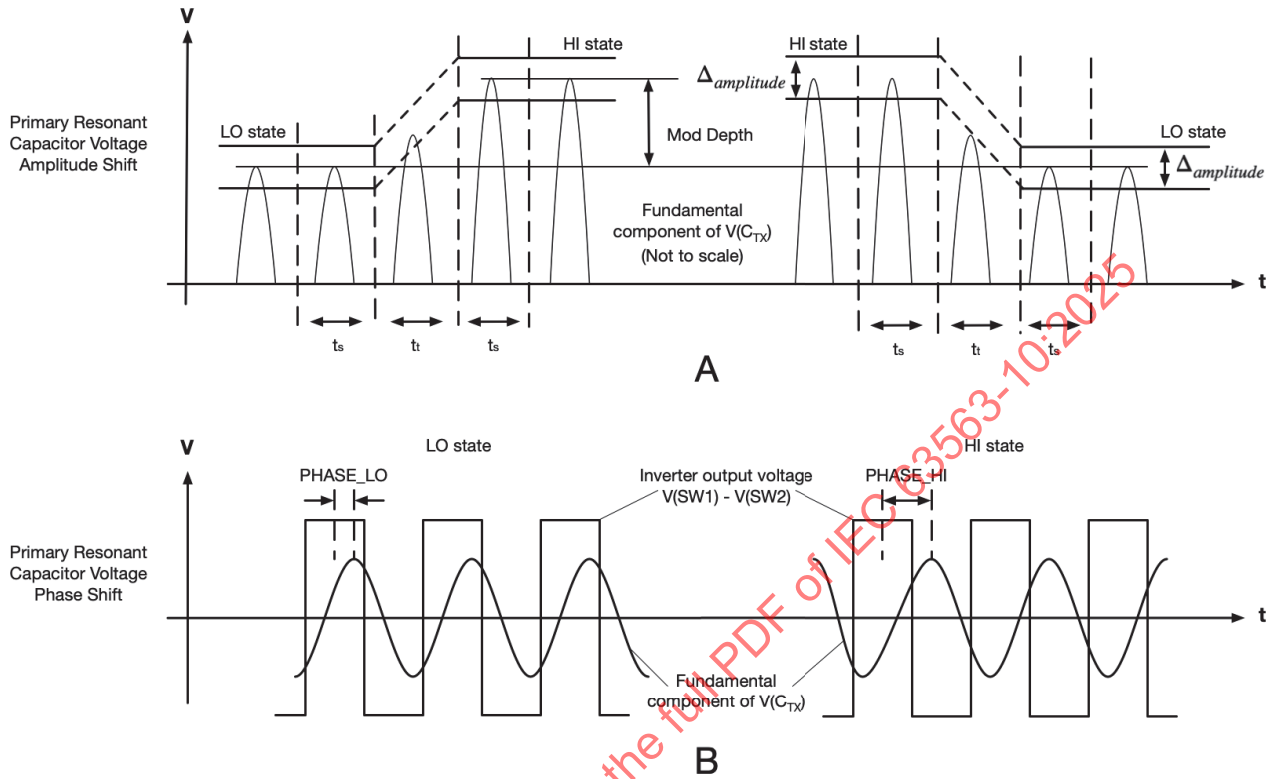
Similar to the Qi specifications defined in Section 2.1 of the Qi Communications Physical Layer Specification v2.0, the system model of the MPP Power Receiver modulates the amount of power it draws from the power signal, such that the primary resonant capacitor voltage at the MPP Power Transmitter assumes two states.

A state may be expressed in terms of magnitude or phase. A state is characterized by the magnitude and/or phase being constant - within a certain ripple band Δ - for at least time $t_s = 100 \mu s$. The magnitude states, M_{HI} and M_{LO} , are measured as the amplitudes (from zero to peak) of the fundamental component of the capacitor voltage. The phase states, P_{HI} and P_{LO} , are measured as the phase angle between the fundamental component of the primary inverter voltage and the fundamental component of the primary resonant capacitor voltage.

These definitions are illustrated in Figure 6.3.1: 66 .

When operating at 360 kHz, the MPP Power Receiver must modulate using real power modulation only. Capacitive modulation will *not* meet this requirement.

Figure 6.3.1: 66 (a) Primary Resonant Capacitor Amplitude and (b) Primary Resonant Capacitor Phase Shift .



5.3.2 System Model

5.3.2.1 ASK Modulator (PRx)

The system model PRx circuit topology is presented in Figure 6.3.2.1: 67 and in Figure 6.3.2.1: 68 . In general, the PRx switches some modulating circuit on and off to change the power drawn from the PTx using ASK.

In accordance with § 5.6.2.7.1 , the ballast load is set to 50 mA.

When operating at 128 kHz, the PRx performs ASK modulation by switching 33 nF $\pm 10\%$ X7R communications capacitors from AC1 and AC2 to ground. The communications switches:

- are subject to a peak stress of approximately $2(V_{RECT} + \text{diode drop})$ (also applies to communications capacitors)
- are turned on with zero voltage switching to avoid unnecessary transients
- are turned off immediately to avoid unpredictable behavior at light load.

When operating at 360 kHz, the PRx communicates as follows by switching electronic load current from V_{RECT} to ground. The modulator:

- switches between two currents - for modulator on and modulator off - with a difference MOD_DEPTH of approximately 50 mA

- the modulator begins in the ON state to help stabilize V_{RECT} before communications begin
- the modulator current in the OFF state, MOD BASE, is adjustable, and selected per Table 6.3.2.1: 19.

Note: the exact MOD_DEPTH and MOD_BASE currents required for successful communication will vary with the PRx operating conditions. At lighter loads, increasing MOD_BASE can improve signal quality (i.e. SNR). When the PRx load fluctuates, increasing MOD_DEPTH can improve signal amplitude. It may be appropriate to dynamically adjust MOD_DEPTH and/or MOD_BASE during operation to maintain communications.

Table 6.3.2.1: 19 Selection of MOD_BASE.

Operating Mode	V _{RECT_TARGET}	Load Current	MOD_BASE	Benefit
Power Transfer	14 V		0 mA	
Power Transfer	12 V	≥ 595 mA	0 mA	
Power Transfer	12 V	< 595 mA	70 mA	mitigates V _{RECT} rise if load dump occurs
Others			70 mA	improves quality of communications signals

Figure 6.3.2.1: 67 System Model for ASK Modulator at 128 kHz .

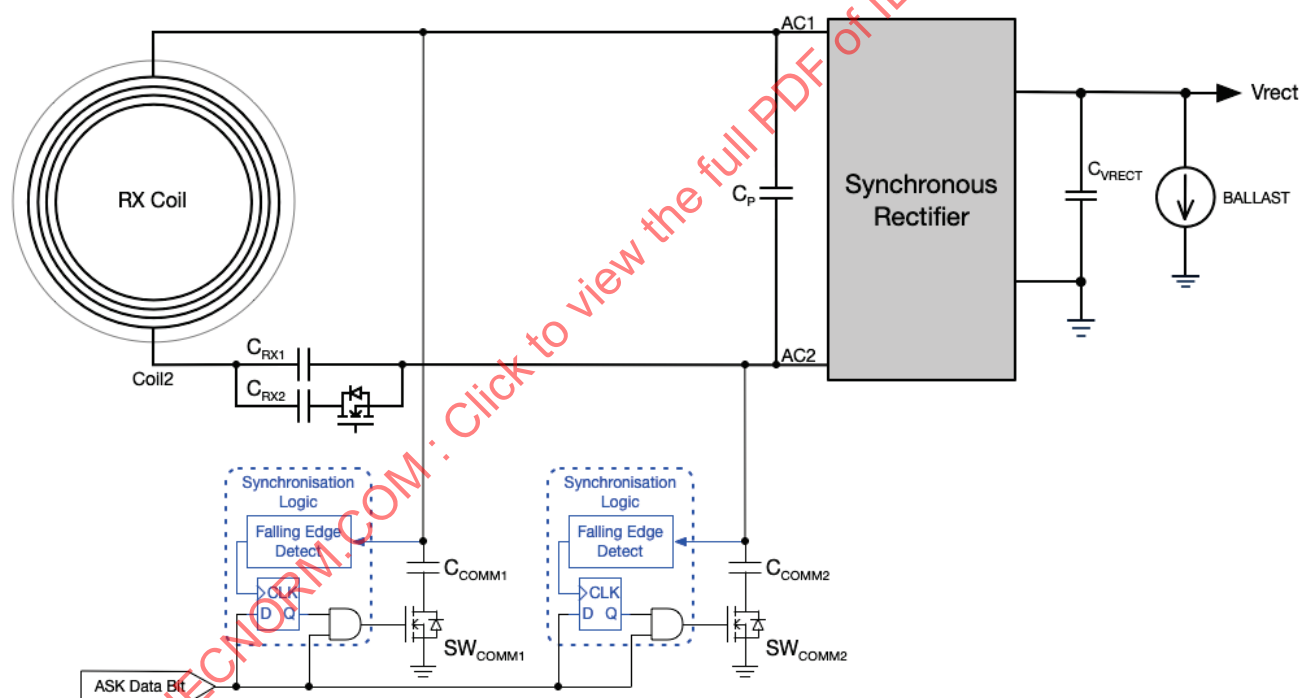


Figure 6.3.2.1: 68 System Model for ASK Modulator at 360 kHz .

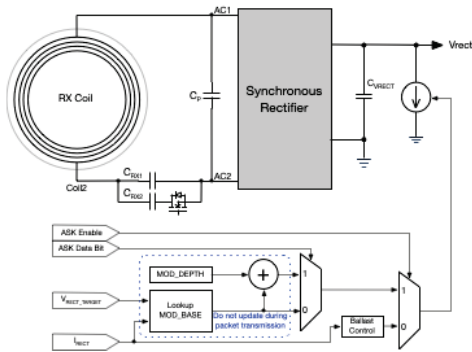
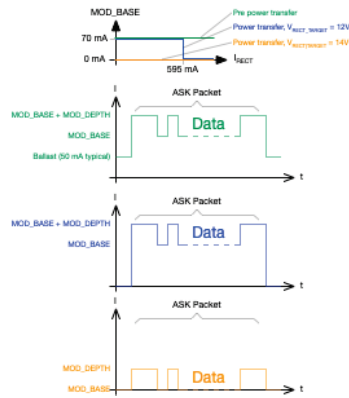


Figure 6.3.2.1: 69 Representative Waveforms for ASK Modulator at 360 kHz .



5.3.2.2 ASK Receiver (PTx)

The system model of a PTx ASK receiver is presented in Figure 6.3.2.2: 70 .

In general, the PTx measures the voltage across the transmitter series capacitor using a differential amplifier, analog anti alias filter and fast ADC. The intent of this circuitry is to digitize the power frequency signal up to a bandwidth of at least 360 kHz. The ADC requires a resolution of ≥ 10 bits and a sampling rate ≥ 10 times f_{OP} .

The ADC results are then processed in the digital domain:

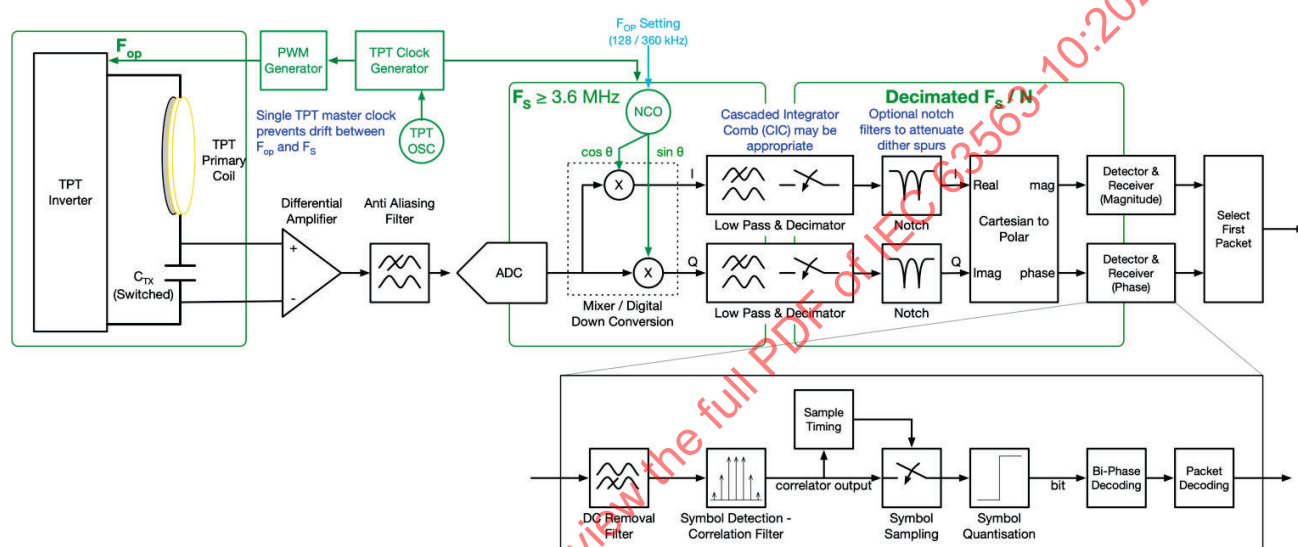
- a quadrature demodulator frequency-shifts the ADC output signal from f_{OP} to near DC. The frequency range of interest is reduced from > 360 kHz to around 10 kHz. The demodulator outputs a complex signal, consisting of an In-phase component I and a Quadrature-phase component Q
- a low pass filter and decimator reduce the sampling rate from the ADC rate - some MHz - to an intermediate data rate - some 10s of kHz. A Cascaded Integrator Comb (CIC) filter may be used here to efficiently filter and decimate the signal, but other methods are available
- the I and Q signals are converted to Magnitude and Phase signals
- the Magnitude and Phase signals are each connected to independent detector / receiver units
- finally, the receiver takes whichever is available - and correct - first from the Magnitude and Phase detector / receiver units.

The detector / receiver units:

- may be implemented in hardware, software, or a mixture of the two
- remove DC content from the input signal (whether Magnitude or Phase)
- apply symbol detection filters; these detect the specific shape of ASK signal waveforms and remove as much noise as possible
- apply some form of sample timing control. Numerous methods can be used, such as:
 - peak detection and timing
 - clock recovery using a Phase Locked Loop
- sample the incoming data stream to produce a stream of individual encoded bits
- remove the differential bi-phase encoding
- packet decoding.

Note: a significant advantage of the above approach is that ADC samples are, in effect, averaged over time. This reduces the impact of system noise, especially switching transients from PTx inverter operation.

Figure 6.3.2.2: 70 System Model for ASK Receiver .



5.3.2.3 ASK Modulation Trends

The signals measured at the MPP Power Transmitter depend upon both the operating power level and the modulation method used. Figure 6.3.2.3: 71 illustrates - in approximate terms - how a DC load current or switched capacitor modulator produces different results as the power flow varies.

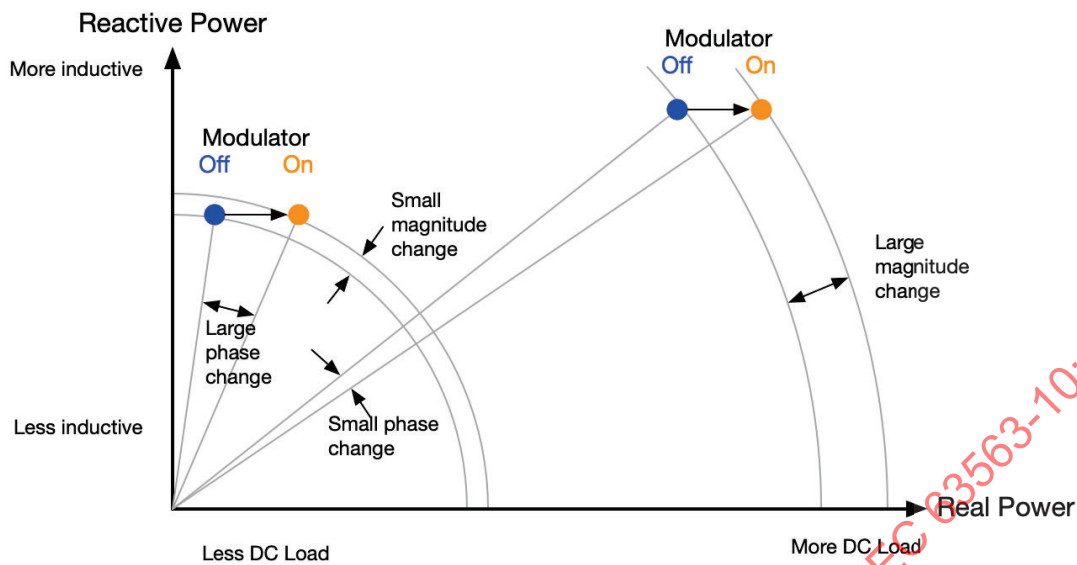
At light load, the power flow out of the Power Transmitter's inverter is largely reactive. DC load changes the real power consumption, resulting in a smaller change in the magnitude signal and a larger change in the phase signal. Conversely, capacitor modulation changes the reactive power consumption, resulting in a larger change in the magnitude signal and a smaller change in the phase signal.

Because the current version of this specification requires a Power Receiver to use of real power modulation at 360 kHz, an ASK receiver which is only sensitive to the magnitude of a given signal (such as the series capacitor voltage or coil current) inside the Power Transmitter may not perform well at light loads.

At heavy load, the power flow out of the Power Transmitter's inverter is largely real. DC load changes the real power consumption, resulting in a larger change in the magnitude signal and a smaller change in the phase signal. Conversely, capacitor modulation changes the reactive power consumption, resulting in a smaller change in the magnitude signal and a larger change in the phase signal.

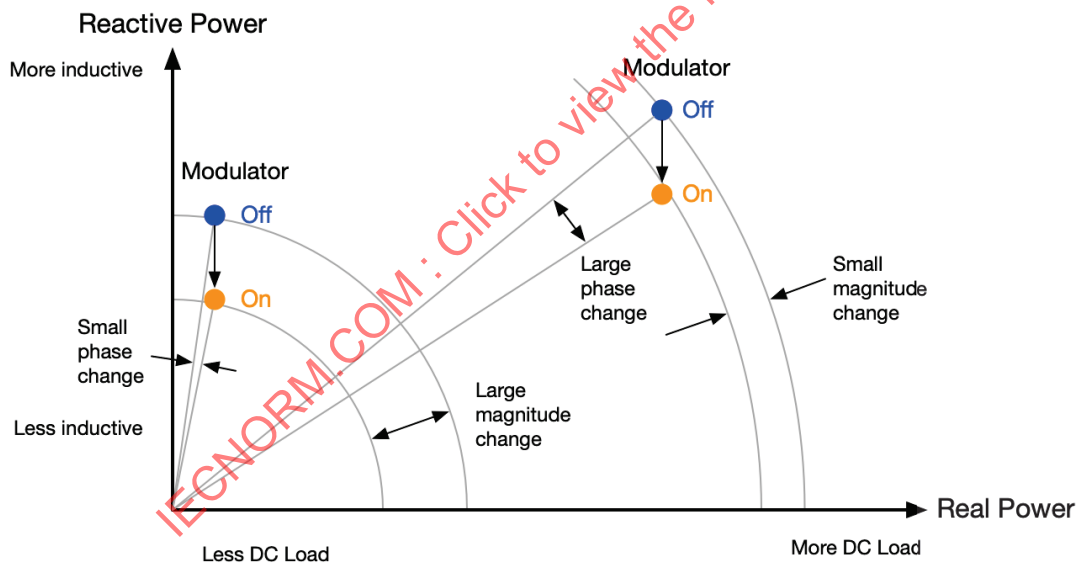
Figure 6.3.2.3: 71 ASK Modulation Trends for (a) DC Load Current and (b) Capacitor Modulation .

DC Load Current Modulation



A

Capacitor Modulation



B

5.3.3 ASK Specifications

This section details the amplitude modulation specifications for MPP PTx and PRx.

It is acceptable for a Power Receiver to meet the amplitude modulation set in some positions (or loads) and meet the phase modulation set in other positions (or loads) provided that at least one is met in every combination of positions and load.

While the Power Receiver is required to only implement real power modulation at 360 kHz, the Power Transmitter is required to be sensitive to all listed modes of modulation.

Note: the requirement for the Power Receiver to use real power modulation at 360 kHz is an interim measure to provide confidence in the interoperability of Power Transmitters and Receivers. It has been shown that the use of switched capacitors for ASK modulation can, in some combinations, result in minimal or even zero amplitude *and* phase modulation; this causes communications failure.

Note: The requirement for the Power Transmitter to be sensitive to real (DC load, switched resistor) *and* reactive (switched capacitor) modulation methods is intended to allow a future revision of the MPP specification to allow complex (i.e. real and/or reactive) power modulation for ASK.

Section	Specification	Description
6.3.3.1	PRx ASK Spec 1	The MPP Power Receiver shall transmit signals to the Power Transmitter using the same bit encoding scheme as defined in Section 3.2 of the Qi Communications Physical Layer Specification v2.0. To guarantee acceptable decoding the noise injected on the inverter rail should be less than ± 30 mV across the 1 - 8 kHz frequency range.
6.3.3.2	PRx ASK Spec 2	The MPP Power Receiver shall transmit data to the Power Transmitter using the same byte encoding scheme as defined in Section 2.3 of the Qi Communications Physical Layer Specification v2.0.
6.3.3.3	PRx ASK Spec 3	The Power Receiver shall transmit data packets to the Power Transmitter using the same range of preamble lengths as defined in Section 2.4 of the Qi Communications Physical Layer Specification v2.0.
6.3.3.4	PRx ASK Spec 4	The MPP Power Receiver shall transmit data packets to the Power Transmitter using the same header field as defined in Section 2.4 of the Qi Communications Physical Layer Specification v2.0.
6.3.3.5	PRx ASK Spec 5	The MPP Power Receiver shall transmit data packets to the Power Transmitter using the same message field as defined in Section 2.4 of the Qi Communications Physical Layer Specification v2.0.
6.3.3.6	PRx ASK Spec 6	The MPP Power Receiver shall transmit data packets to the Power Transmitter using the same checksum field as defined in Section 2.4 of the Qi Communications Physical Layer Specification v2.0.
6.3.3.7	PRx ASK Spec 7	The MPP Power Receiver shall transmit adjacent bytes within a data packet such that the stop bit of the preceding byte is immediately followed by the start bit of the following byte.
6.3.3.8	PRx ASK Spec 8	When operating at 360 kHz, the MPP Power Receiver shall transmit ASK data by varying its real power load.
6.3.3.9	PRx ASK Spec 9	When the MPP Power Receiver is placed on the Test Power Transmitter TPT#MPP1 within the 2x2 mm MPP cylinder and operating at 128 kHz, at least one of the following conditions shall be met: <ul style="list-style-type: none"> An amplitude difference between M_{HI} and M_{LO} (peak amplitude of fundamental component) and a Signal to Noise Ratio (SNR) of at least 220 mV and 13 dB, respectively, OR A phase difference between P_{HI} and P_{LO} (phase shifts of the fundamental component) and a Signal to Noise Ratio (SNR) of at least 3.0° and 17 dB, respectively.
6.3.3.10	PRx ASK Spec	When the MPP Power Receiver is placed on the Test Power Transmitter

Section	Specification	Description
	10	<p>TPT#MPP1 within the 2x2 mm MPP cylinder and operating at 360 kHz, at least one of the following conditions shall be met:</p> <ul style="list-style-type: none"> • An amplitude difference between M_{HI} and M_{LO} (peak amplitude of fundamental component) and a Signal to Noise Ratio (SNR) of at least 300 mV and 19 dB, respectively, OR • A phase difference between P_{HI} and P_{LO} (phase shifts of the fundamental component) and a Signal to Noise Ratio (SNR) of at least 3.0° and 17 dB, respectively.
6.3.3.11	PTx ASK Spec 1	The MPP Power Transmitter shall receive and decode ASK transmissions from the Power Receiver.

IECNORM.COM : Click to view the full PDF of IEC 63563-10:2025

6 Foreign Object Detection

6.1 Background

MPP uses a two-step approach to foreign object detection (FOD). The most common situation in which an FO arrives between the PTx and PRx is if it is placed on the PTx first (sequential placement of FO). Compared with the case where the FO is placed simultaneously with the PRx, the user is more easily exposed to an over-heated FO if power delivery starts. When the FO is placed on the PTx prior to placement of the PRx it can easily be detected using an § 7.2 Open-air Q-Test (pre-power transfer FOD method) which is executed during the analog ping phase. Because the open-air Q test is so accurate and is not affected by the presence of a PRx, it can be used to guarantee there is no FO which will over-heat even at maximum power delivery.

In the case that the FO arrives with the placement of the PRx, the open-air Q test is no longer able to distinguish FO from PRx. In this situation, the § 7.3 MPP Power Loss Accounting (in-power transfer FOD method) is used for FO detection. Accurately detecting the presence of an FO during power transfer is a challenging task. It may be the case that FO detection which is completely dependent on in-power transfer FOD will have to limit the power transfer to something lower than maximum.

The following table summarizes any power limitations that occur depending on the result of the open-air Q test.

Open-Air Q Test	Result
Not implemented	Limit maximum power delivery to the level supported by § 7.3 MPP Power Loss Accounting (in-power transfer FOD method) alone and set the § 7.3.7 FO Detection Thresholds to the IEC62368 compliance level.
PRx placed on PTx prior to power being applied to PTx	
FO arrives with PRx	
FO detected on PTX	
No FO detected	Allow maximum power delivery.

6.2 Open-air Q-Test (pre-power transfer FOD method)

6.2.1 Introduction

This section introduces a pre-power foreign object detection (FOD) method that is useful for detecting foreign objects placed on the PTx mat prior to the arrival of the PRx.

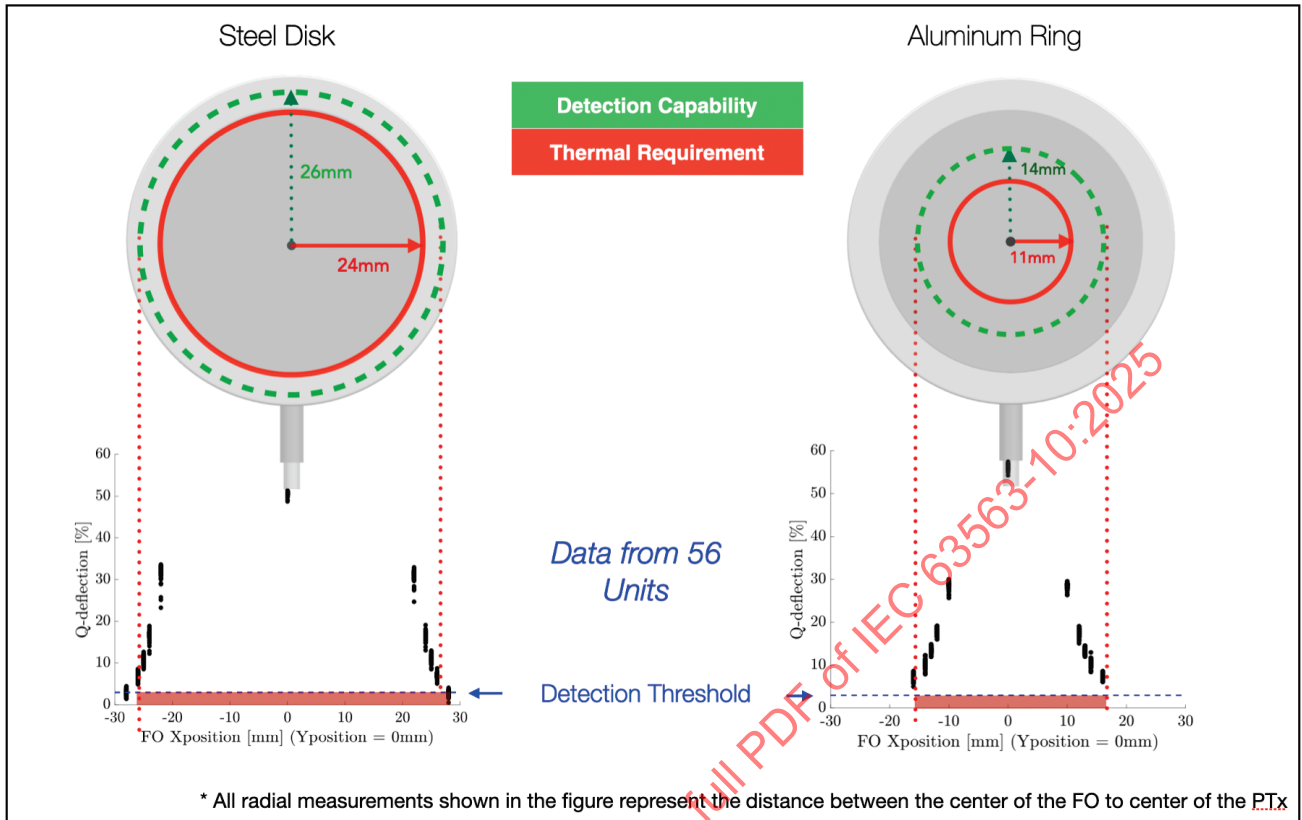
This open-air Q test is not a substitute for in-power transfer FOD, nor a mated-Q method. The open-air Q test will not detect FOs which arrive on the PTx simultaneously with the PRx, or if the FO is inserted in the power transmitter's field after the PRx has arrived.

The basic functionality of the additional method described in this document consists in comparing the response to an analog ping when PTx is running, with the stored-in-unit response to analog ping when PTx is in free air.

During the start-up phase, the PTx uses analog ping to measure a deflection to Q defined as:

$$\Delta Q = 1 - \frac{Q}{Q_0} \quad \text{eq. 3}$$

Figure 7.2.1: 72 Detection Capability V.S. Thermal Requirements .

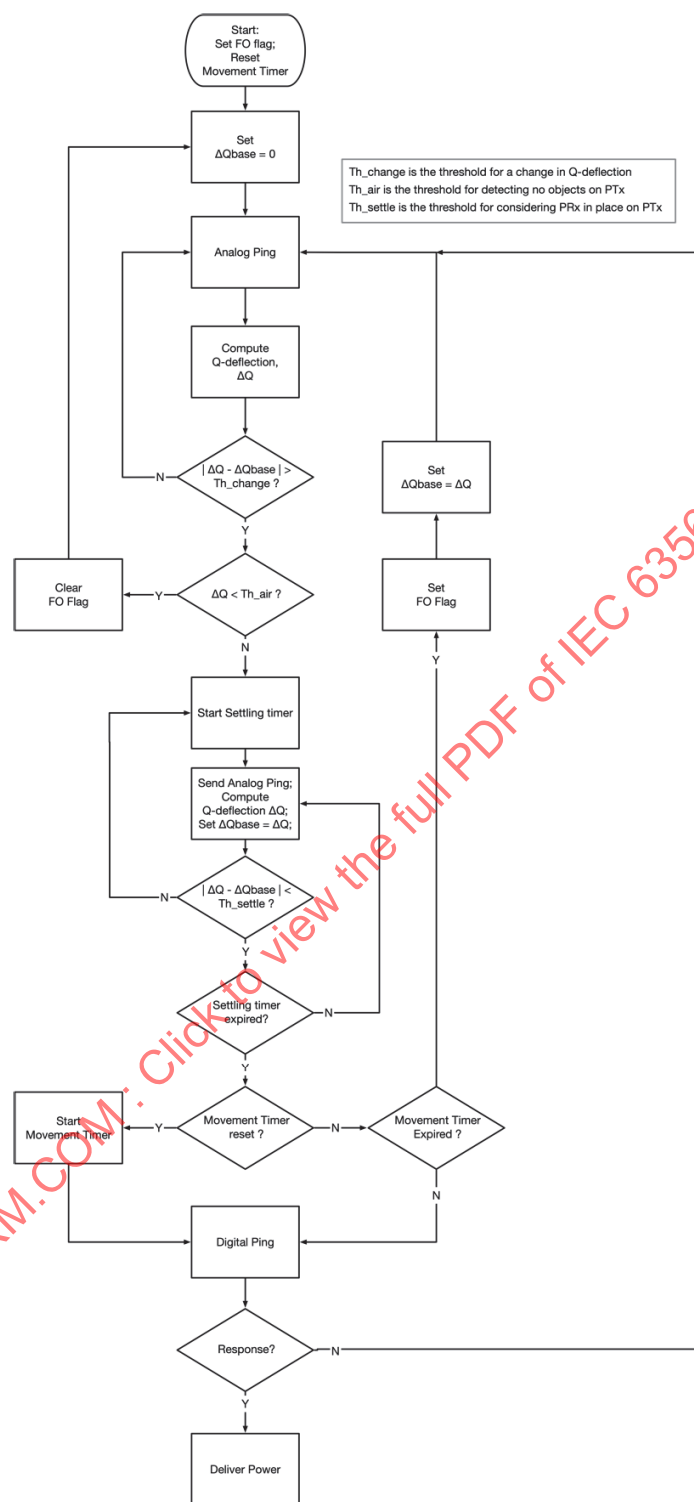


where Q_0 is the calibrated value for open-air Q measured at production and Q is measured by analog ping or calculated from a direct impedance measurement at run-time. Note that $\Delta Q_0 \approx 0$ if there is no FO present, but it's not exactly zero because of effects such as temperature drift as discussed later in this document. Component aging will also cause $\Delta Q_0 \neq 0$ when PTx is operating in free air.

When an object is placed on the mat, the Q will be deflected by some amount. If ΔQ is large enough, an object can be inferred. A response from digital ping can then be used to distinguish between whether an FO or a power receiver was placed on the mat. A basic flow is provided in Figure 7.2.1: 73 .

If open-air test is not implemented, the open-air FO flag should be set so that the in-power FOD method knows that the open-air FO test did not detect the mat clear of FOs. The power contract with PRx should be negotiated to the maximum power that in-power FOD can guarantee with no FO over-heating.

Figure 7.2.1: 73 Simplified flow diagram for open-air Q test .



6.2.2 Movement Timer

In the Q-test flow diagram, a movement timer is set once a Q deflection is detected. While this timer is running, analog pings continue until either (a) a response to the digital ping occurs indicating the presence of a receiver or (b) the movement timer expires. The purpose of the movement timer is to prevent a receiver placed far enough off-center to be falsely detected as an FO while the user is sliding the receiver into place. False detection of FO could happen in such a scenario because the Q-deflection is quite sensitive, more so than digital ping.

The duration of the movement timer should be 1 - 2s. Because of the magnet attach, the receiver will snap into place very quickly. More information about the movement time is provided in § 7.2.6.4.2 PRx misplaced then replaced .

6.2.3 Settling Timer

Because the § 5.7 K Estimation occurs after successful digital ping, it is important for digital pings to commence only after the Q deflection has settled. The Q deflection being settled indicates that the PRx is now in position and no longer moving. More information is provided in § 7.2.7 PRx movement and digital ping .

6.2.4 Glossary

Table 7.2.4: 20 Glossary .

Glossary		
Acronym	Term	Description
FO	Foreign Object	
PTx	Transmitter	
PRx	Receiver	
	Critical Radius	Distance from the center of the coil that defines the area within which an FO will heat up beyond its temperature limits (70°C for RFO#MPP1) when PTx transfers the maximum rated power to a PRx at any position within the active volume at that power. The Critical radius depends on the type of Foreign Object
	Q-deflection	Variation of the Q-factor of PTx from its value when in free air
	Qtest	Algorithm that calculates Q-deflection

6.2.5 Open-air Q-Test Specifications

Section	Specification	Description
7.2.5.0.1	PTx Q-Test Spec 1	If implemented, the open-air Q test should detect the presence of a Foreign Object within the area defined by the critical radius before power transfer begins
7.2.5.0.2	PTx Q-Test Spec 2	If implemented, the open-air Q test should be performed periodically during PTx standby with a maximum period of 1 Qtest/s
7.2.5.0.3	PTx Q-Test Spec 3	If implemented, the Q-factor and the natural frequency of the LC tank of the PTx in free air should be known to PTx to calculate the Qdeflection with open-air Q test

Section	Specification	Description
7.2.5.0.4	PTx Q-Test Spec 4	If implemented, PTx should try to initiate communication (via digital ping) when Q-deflection (ΔQ) is higher than free air threshold ΔQ_{th}
7.2.5.0.5	PTx Q-Test Spec 5	If implemented, A FO flag should be set if communication fails after digital ping is sent
7.2.5.0.6	PTx Q-Test Spec 6	If implemented, a FO flag should be set if the open-air Q test is not performed
7.2.5.0.7	PTx Q-Test Spec 7	If implemented, a FO flag should be set if an FO within the critical radius is detected
7.2.5.0.8	PTx Q-Test Spec 8	If implemented, a FO flag should be set if PTx has not measured Q-deflection (ΔQ) below free air threshold (ΔQ_{th}) prior to receiving the digital ping response.
7.2.5.0.9	PTx Q-Test Spec 9	If implemented, a FO flag should be cleared if and only if PTx has measured Q-deflection (ΔQ) below free air threshold (ΔQ_{th})
7.2.5.0.10	PTx Q-Test Spec 10	If implemented and the FO flag is set, the maximum power capability should be set based on FOD capability of the in-power FOD method to prevent the FO from heating up beyond the temperature limit associated with that object and placement sequence.
7.2.5.0.11	PTx Q-Test Spec 11	If implemented, the maximum R_{AC} (total resistance in free air) of the MPP PTx should be limited to: $R_{AC} \leq \Delta R_{FO} \left(\frac{1}{\Delta Q} - 1 \right)$ Given the resistance variation caused by the FO (ΔR_{FO}) and a desired ΔQ .

6.2.6 Theory of Operation

6.2.6.1 Measuring Q

In this approach, a pulse of energy is injected into the coil and the decay of the ringing response is measured. Q is then estimated from the decay envelope. See *Estimate Q from the decay of the ringing response to a pulse* from Annex B, FOD Book, Qi Specification v2.0.

Figure 7.2.6.1: 74 Implementation of how to measure ring response .

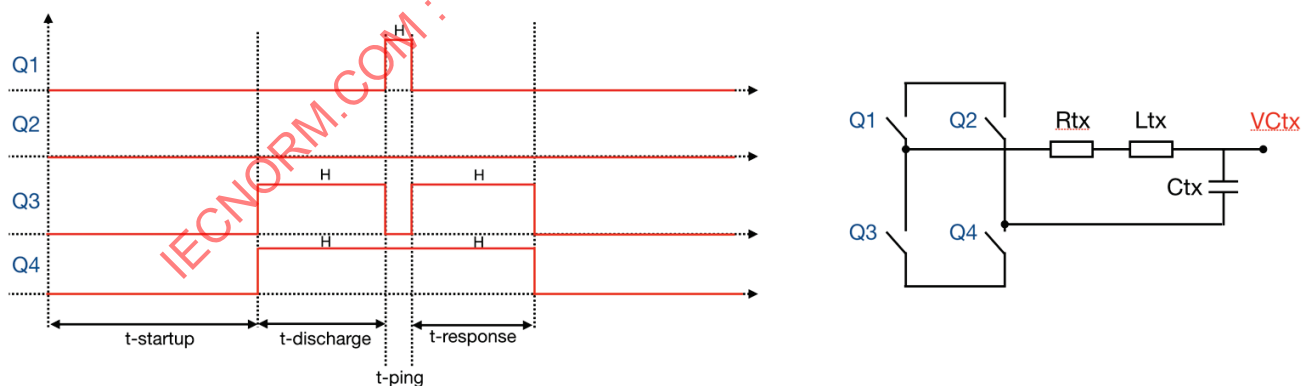


Figure 7.2.6.1: 74 shows a possible implementation by driving the FETs of the inverter. The different phases can be described as:

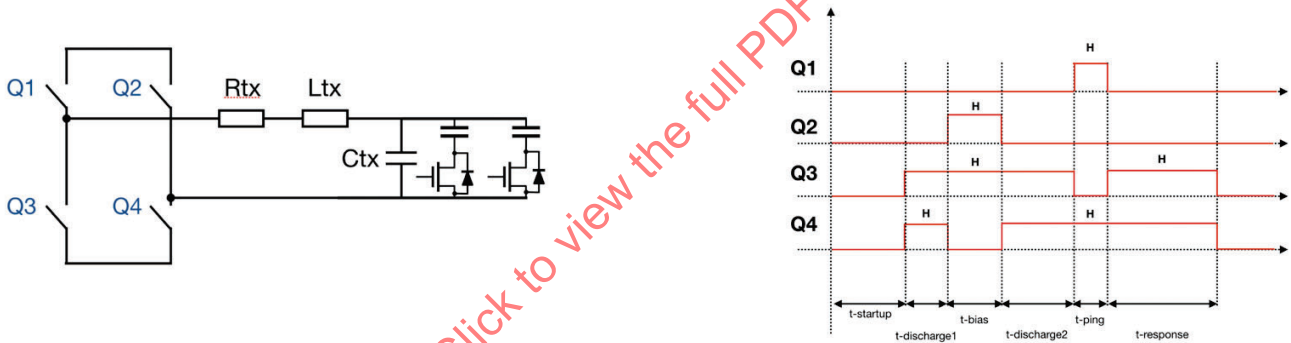
1. **t-startup**
During this time, the input voltage of the inverter is allowed to reach the required nominal voltage for the ping.
2. **t-discharge**
The purpose of this stage is to discharge the resonant capacitor and to establish the initial conditions for the ping (i.e. $V_{Ctx}(0) = 0$, $i_{Ltx}(0) = 0$). This should be done by shorting the resonant tank via the bottom switches of the inverting bridge (e.g. Q3 and Q4).
3. **t-ping**
This is the energy injection stage. During this stage, the DC source is connected across the Tx resonant tank for t-ping time. This should be done by turning off Q3, turning on Q1, and leaving Q4 on as shown in Figure 7.2.6.1: 74 .
4. **t-response**
After energy is being injected into the tank during the ping stage, the tank should be shorted via the low side switches to allow for free oscillation of the resonant tank. This should be done by turning off Q1 and turning on Q3. The natural response of the tank (e.g. the voltage across the Tx tuning cap) is then sampled and processed.

Estimating Q requires accurate sampling of the waveform peaks to obtain its envelope. To eliminate the impact of the DC offset from the decay estimate the envelope amplitude can be measured as the peak-to-valley difference. Please refer to Annex B.2, FOD Book, Qi Specification v2.0.

6.2.6.1.1 Note on PTx with multiple resonant capacitors

When not all resonant capacitors are used, a negative bias voltage is required to pre-charge the unused capacitors via the body diode(s) of cap the selection FET(s). After the pre-charge phase, another discharge phase is required to discharge the capacitors that will be used during the ping phase. See Figure 7.2.6.1.1: 75 .

Figure 7.2.6.1.1: 75 bias ping configuration .



6.2.6.1.2 Impact of FO or PRx on Q-deflection

Please refer to Annex B3, FOD Book, Qi Specification v2.0.

6.2.6.2 Q compensation for drift

This section provides some possibilities for improving the Q deflection measurement which may or may not be needed for some implementations. The Q deflection in eq. 3 is intended to compare the run-time measurement of Q against the production calibrated measurement of Q. During run-time, effects besides the presence of an FO such as temperature and frequency drift can result in Q deflection. Compensating for these effects improves the reliability of the open-air Q test.

6.2.6.2.1 Accentuating Q deflection due to frequency drift caused by FO

Please refer to Annex B4, FOD Book, Qi Specification v2.0.

6.2.6.2.2 Temperature Compensation

Please refer to Annex B6, FOD Book, Qi Specification v2.0.

6.2.6.2.3 Separating DC and AC resistance

Many drift effects in the measurement of Q occur to the DC portion of the resistance (frequency independent) which, itself, is not affected by the presence of an FO. Frequency independent “DC resistances” include resistances from the PCB traces and inverter FET resistances. If the DC resistance is separated from the overall resistance, the DC resistance can be calibrated at production and remove the impact of DC resistance drift. Specifically, let:

$$R = R_{DC}(T) + R_{coil,AC}(T, \omega) \quad \text{eq. 4}$$

where we've indicated that $R_{DC}(T)$ is sensitive to temperature while $R_{coil,AC}(T, \omega)$ is sensitive to temperature and frequency.

Using eq. 4, Q can be written as:

$$Q = \frac{\omega L}{R} = \frac{\omega L}{R_{DC} + R_{coil,AC}} \quad \text{eq. 5}$$

The total resistance, R , can also be determined by the analog ping ringing response:

$$L = \frac{1}{2\pi F_r^2 C} \quad \text{eq. 6}$$

$$R = \frac{2\pi F_r L}{Q} \quad \text{eq. 7}$$

$$R_{coil,AC} = R - R_{DC} \quad \text{eq. 8}$$

If the DC resistance is measured, its value, $R_{DC,0}$, can be stored at production and then compute Q at run-time as:

$$Q_{comp} = \frac{\omega L}{R_{DC,0} + R_{coil,AC}} = Q \cdot \frac{R}{R_{DC,0} + R_{coil,AC}} \quad \text{eq. 9}$$

This effectively eliminates DC drift from the Q measurement at the cost of additional measurement error of the resistances.

Finally, replace eq. 3 with:

$$\Delta Q = 1 - \frac{Q_{comp}}{Q_0} \quad \text{eq. 10}$$

To achieve a Q deflection of 10%, the PTx AC resistance should be no more than ~216mΩ. If the PTx can measure Q more accurately, it can afford to have a higher AC resistance.

6.2.6.3 Choosing a Q deflection threshold

Please refer to Annex B5, FOD Book, Qi Specification v2.0.

6.2.6.4 Potential Implementation Issues

6.2.6.4.1 Proximity to metal objects

Please refer to Annex B.7, FOD Book, Qi Specification v2.0.

6.2.6.4.2 PRx misplaced then replaced

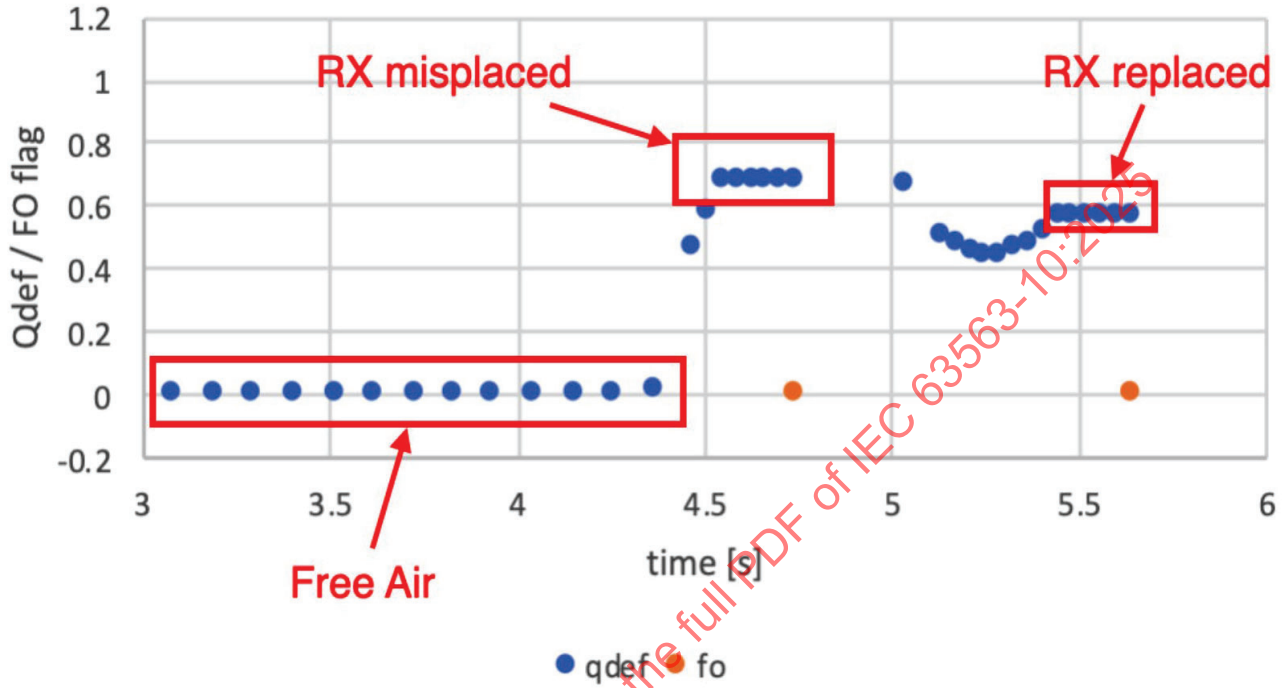
In case of PRx misplacement (e.g. placing the PRx on PTx then sliding it to a correct position) an FO flag could be set, consequently, PTx could inhibit power transfer or start power transfer at a reduce power rate when PRx is then placed on a

correct position.

To mitigate this issue, a possible § 7.2.2 Movement Timer could be introduced as shown in Figure 7.2.1: 73 .

The mitigation consists in delaying the FO flag in an attempt to establish communication before the movement timer expires as shown in Figure 7.2.6.4.2: 76 .

Figure 7.2.6.4.2: 76 PRx replaced before the movement timer expires to prevent false FO flag .



6.2.6.5 Summary

The open-air Q test is used to calculate the Q-deflection.

Q-deflection measures the variation of the Q-factor during run time from its value when in free air (unmated and with no Foreign Objects):

$$\Delta Q = 1 - \frac{Q}{Q_0}$$

- ΔQ is Q-deflection
- Q is the Q-factor calculated in-field during run time operation, this parameter could be compensated for R_{AC} drift due to aging and/or temperature
- Q_0 is the Q-factor in free air and it could be stored in the unit during production

At the critical radius, the Q-deflection is defined as follows (assuming $\Delta L_{FO} = 0$):

$$\Delta Q_{critical} = 1 - \frac{R_{AC}}{R_{AC} + \Delta R_{FO}}$$

- R_{AC} is total resistance of the coil and everything else in the path of Q measurement (e.g. FET switches, PCB traces, cap ESR).
- ΔR_{FO} is the variation of R_{AC} due to the presence of a FO at the critical radius

- ΔL_{FO} is the variation of L_0 (inductance in free air) due to the presence of a FO at the critical radius

The Q-deflection threshold should have enough margin to account for measurement error and component aging:

$$\Delta Q_{th} \leq \Delta Q_{critical} - d_{aging} - e_{error}$$

- ΔQ_{th} is the Q-deflection threshold
- $\Delta Q_{critical}$ is the Q-deflection value when a Foreign Object is placed at the critical radius
- d_{aging} is the Q-deflection drift cause by aging
- e_{error} is the Q-deflection inaccuracy introduced by the algorithm used to calculate Q-factor

The Qdeflection threshold could be affected by the proximity to metal object (e.g. PTx placed on a metal table).

6.2.7 PRx movement and digital ping

It has been shown how to choose a Qdeflection threshold based on ΔR_{AC} caused by the presence of a FO. This implies that when PTx detects $\Delta Q > \Delta Q_{th}$ a digital ping will be sent to try to establish communications. PRx could cause a Qdeflection higher than the thresholds while it's approaching PTx, leading to a possible failure to respond to digital ping from PTx or poor coupling estimation. Failing to respond to digital ping leads to setting the FO flag hence possible power transfer limitation.

To avoid this issue, it is possible to introduce a Qdeflection settling period during which the PTx will wait until the computed Qdeflection is settle (PRx not moving) to send a digital ping and try to establish communications.

The following scenario describes a possible implementation of the settling period:

1. PTx is in stand-by mode, calculating ΔQ periodically (e.g. every 100ms)
2. PRx is approaching PTx causing $\Delta Q > \Delta Q_{th}$ while still moving
3. PTx will enter a settling period as soon as $\Delta Q > \Delta Q_{th}$
4. PTx will keep calculating ΔQ (the sampling rate could be increased to improve the resolution)
5. ΔQ is considered settled only if it has not varied beyond $\pm \Delta Q_{settle}\%$ (e.g. 1%) for at least t_{settle} (e.g. 200ms), indicating that the PRx is stationary
6. This settling criterion will ensure that PRx is placed on PTx and a digital ping can be sent.

ΔQ_{settle} and t_{settle} define a minimum PRx placement velocity. This is required to avoid sending a digital ping prematurely that could affect the coupling estimation.

To calculate the minimum placement velocity, the designer should consider the smallest variation of ΔQ over the area of interest of the PTx.

For instance, let:

$$\frac{dx}{dQ} \text{ variation of } \Delta Q \text{ over x-axis of the PTx}$$

The minimum required velocity to avoid premature settling is:

$$v_{min} = \frac{\frac{dx}{dQ} \times \Delta Q_{settle}}{t_{settle}}$$

please note that ΔQ_{settle} needs to be as small as possible and it's limited by noise, algorithm inaccuracy and possible interactions with PRx.

A possible scenario:

$$\frac{dx}{dQ} = 1.0406 \text{ mm}/\%$$

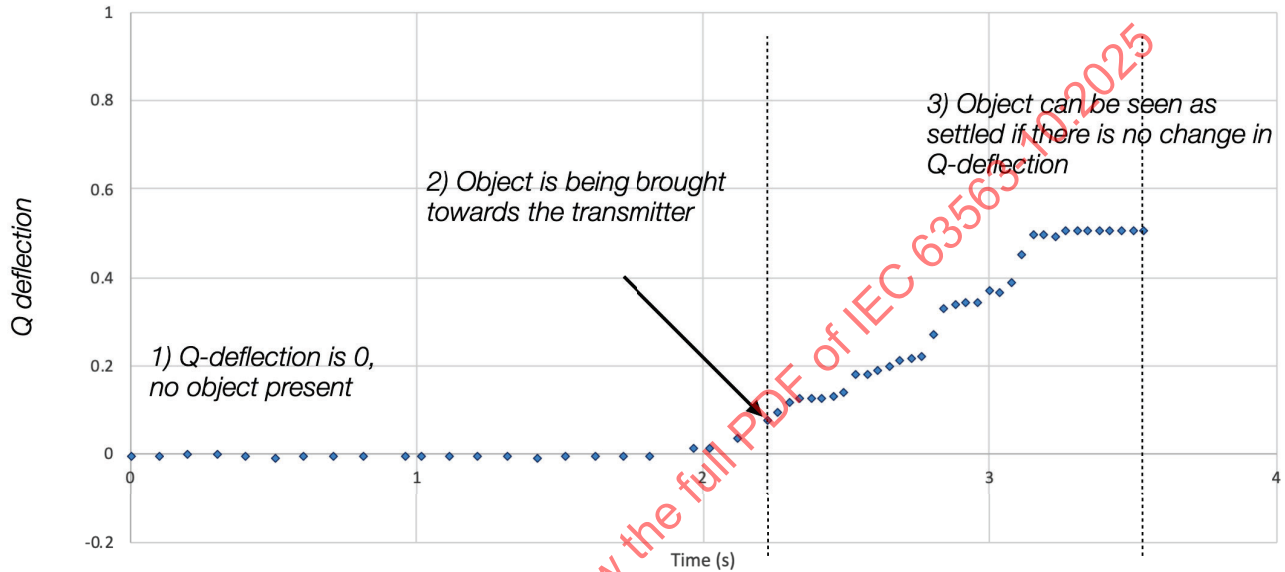
$$\Delta Q_{settle} = 1\%$$

$$\Delta t_{\text{settle}} = 187.5 \text{ ms}$$

$$v_{\text{min}} = 5.55 \text{ mm/s}$$

Figure 7.2.7: 77 shows an example of what Q-deflection looks like when PRX is approaching PTX. During (1) the Q-deflection is 0% and at (2) the Q-deflection has exceeded the threshold. The sampling rate could be increased once $\Delta Q > \Delta Q_{th}$ to improve the resolution. At (3) the Q-deflection has not changed for the minimum required time therefore a digital ping can be sent and power transfer can begin.

Figure 7.2.7: 77 Example of q-deflection profile when Prx is approaching PTx .



6.3 MPP Power Loss Accounting (in-power transfer FOD method)

6.3.1 Introduction

Qi v1.1 introduced power loss accounting for in-power transfer foreign object detection. Modifications are introduced here to extend power loss accounting to 15W power delivery and beyond, without the need for run-time re-calibration. This enhanced approach will be referred to as "MPP Power Loss Accounting" (MPLA).

The approach offered for MPLA is based on the following:

- MPLA is designed to ensure adequate accuracy so that 15W can be delivered in the $r=[0,2\text{mm}]$, $z=[0,2\text{mm}]$ (the "2x2 cylinder", see § 2.3.1 Definitions) state-space without over-heating an FO in order to meet the requirements of IEC62368-1:2018 section on thermal burn injury requirements for wireless power transmitters.
- The loss error is designed to increase (or at least be non-negative) as PRx position displacement increases from the coil's center. In this way, displacements outside the 2x2 cylinder, MPLA will be biased towards false FO detection and power throttling versus missed FO detection which would allow FO heating to exceed temperature limits.

- Coil and friendly metal losses (see Figure 7.3.5: 79 below), strongly dependent on mated coupling properties (LQK²), are separated from circuit losses outside the magnetic circuit.
- Friendly metal losses are accounted separately from coil losses using the power loss split model § 8.3 Loss-Split Modeling: A framework for calculating localized eddy-current losses .
- The loss error is computed for a reference design pair (TPT#MPP1 - TPR#MPP1) using equations and coefficients accounting for the coil and friendly metal which are provided in this chapter.
 - The reference design units represent exemplary MPP designs
 - Performance of the error between arbitrary mated PTx to PRx designs is ensured by exchanging eco-system scaling parameters during the negotiation stage prior to power delivery and by (a) ensuring that the reference designs provide adequate performance when mated to each other and (b) by choosing the eco-system scaling coefficients to translate the mated PTx to PRx inductive properties (LQK) to the LQK of the reference designs.
 - MPLA error compliance is evaluated for the PTx or PRx coupled to the high-accuracy test tools which are closely matched to the MPP reference designs.
- The basic power accounting approach in BPP biases the PRx loss estimate to always over-estimate the loss (Test #57: Delta Pr error from -0 to +350 mW). This bias is unknown to the PTx but the PTx needs to compensate for it in its power loss calculation. In MPLA, both the PTx and PRx should have a zero-mean power estimates so that computed P_{FO} is zero-mean within the 2x2 cylinder.
- Power contract re-negotiation is provided to allow power to be reduced in the presence of an FO to prevent over-heating (“best effort charging”).

6.3.2 MPLA Specifications

6.3.2.1 MPLA PRx Specifications

These are the MPLA specifications for PRx. The pFO limits in PRx specs 5-6 are derived from an error analysis provided in § 7.3.10 Error Budget .

Section	Specification	Description
7.3.2.1.1	PRx MPLA Spec 1	During the Negotiation phase, PRx shall send parameters $g_{coil, TX}$, α_{FM} and $\alpha_{FM, DC}$ to PTx. See Table 7.3.4.1: 22 .
7.3.2.1.2	PRx MPLA Spec 2	During the Negotiation phase, PRx shall request parameter $g_{coil, RX}$ from PTx. See Table 7.3.4.1: 22 .
7.3.2.1.3	PRx MPLA Spec 3	PRx shall negotiate T_{Window} and T_{Offset} according to Qi Communications protocol book, see 8.4 Configuration and set Window size=[01000] ($T_{Window} = 32ms$) and Window offset=[00100] ($T_{Offset} = 16ms$).
7.3.2.1.4	PRx MPLA Spec 4	PRx shall measure its P_{RECT} and calculate its received power (P_{PR}) and send them to the PTx in the PLA packet (0x58).
7.3.2.1.5	PRx MPLA Spec 5	PRx shall send its received power (P_{PR}) and P_{RECT} to PTx in the PLA packet (0x58) when any of the following conditions are met: <ul style="list-style-type: none"> • previous PLA packet was sent more than 2050ms ago (1.5s preferred) [reference: Section 4.3.1. Power Loss Accounting Packet - Timing in <i>MPP Communication Interface</i>] • P_{RECT} is 1W higher than P_{RECT} from the previous PLA packet • the time from receiving “NAK” packet from PTx in response to a PLA packet exceeds 300ms
7.3.2.1.6	PRx MPLA Spec 6	With no FO present, for all PRx positions within the 2x2 cylinder, when $P_{RECT} \leq 10W$, the computed P_{FO} of PRx mated to the TPT#MPP1 shall be within the range [-135mW, +135mW].

² LQK refers to the key electrical observables of the mated inductive coils. The first letter represents the inductive parameters of the mated inductive coils (L'TX and L'RX). The second letter represents the quality factor of the coil (Q'TX and Q'RX). The last letter stands for the coupling factor between the coils, which includes the inductive coupling k_i and the resistive coupling k_r .

Section	Specification	Description
		Note: these values are determined from the § 7.3.10.3 pFO Error Budget .
7.3.2.1.7	PRx MPLA Spec 7	With no FO present, for all PRx positions within the 2x2 cylinder, when $P_{RECT} > 10W$ up to the maximum declared power, the computed P_{FO} of PRx mated to the TPT#MPP1 shall be within the range $[-220mW, +220mW]$. Note: these values are determined from the § 7.3.10.3 pFO Error Budget .
7.3.2.1.8	PRx MPLA Spec 8	Outside of the 2x2 cylinder, the computed P_{FO} shall be positive.
7.3.2.1.9	PRx MPLA Spec 9	Upon receiving "ACK" as a response to a PLA packet, PRx shall ramp its load power to comply with the negotiated value of Guaranteed Power (see § 5.10.3.4.4).
7.3.2.1.10	PRx MPLA Spec 10	When the PRx is ramping its load after receiving an "ACK" response to a PLA packet, it shall limit its load increases to steps of 1W or less.
7.3.2.1.11	PRx MPLA Spec 11	Upon receiving "NAK" as a response to a PLA packet, If V_{RECT} is lower than the target level minus 1.5V, PRx should reduce its load to bring V_{RECT} within - 1.5V / +0.5V of the target.
7.3.2.1.12	PRx MPLA Spec 12	Upon receiving "NAK" as a response to a PLA packet, PRx shall not ramp up its load power (even if P_{RECT} is less than the target power).
7.3.2.1.13	PRx MPLA Spec 13	Upon receiving "NAK" as a response to a PLA packet, PRx shall compute and send a new PLA packet every 250ms - 300ms.
7.3.2.1.14	PRx MPLA Spec 14	$g_{coil, TX}$ should have a value of 1.0.

6.3.2.2 MPLA PTx Specifications

These are the MPLA specifications for PTx. In specs 4, 6, 9, 10, 12 and 14, the TPR is to report PPR_{est} instead of PPR to ensure the PTx MPLA implementation has sufficient margin and FO detection is working as expected. The PPR_{est} values are derived from the § 7.3.10.5 Power Loss Accounting Compliance Testing .

Test scenarios 1 and 2 are described in § 7.3.7 FO Detection Thresholds . In the case that the § 7.2 Open-air Q-Test (pre-power transfer FOD method) is implemented, test scenario 2 corresponds to § 7.2.5 Open-air Q-Test Specifications is not set. Test scenario 1 corresponds to the FO flag being set or the case that the open-air Q test is not implemented.

Section	Specification	Description
7.3.2.2.1	PTx MPLA Spec 1	During the Negotiation phase, PTx shall send parameters $g_{coil, RX}$ to PRx. See Table 7.3.4.1: 22 .
7.3.2.2.2	PTx MPLA Spec 2	During the Negotiation phase, PTx shall receive parameters $g_{coil, TX}$, α_{FM} and $\alpha_{FM, DC}$ from PRx. See Table 7.3.4.1: 22 .
7.3.2.2.3	PTx MPLA Spec 3	With no FO is present, for all TPR positions within the 2x2 cylinder, when TPR#MPP1 is reporting $P_{PR, est} = P_{PR} - 112mW$ and is receiving up to 10W (scenario 1), the PTx shall not apply power throttling nor disconnect due to FO detection nor shut down.
7.3.2.2.4	PTx MPLA Spec 4	With no FO is present, for all TPR positions within the 2x2 cylinder, when TPR#MPP1 is reporting $P_{PR, est} = P_{PR} - 141mW$ and is receiving up to 15W (scenario 2), the PTx shall not apply power throttling nor disconnect due to FO detection nor shut down.
7.3.2.2.5	PTx MPLA Spec 5	With no FO present, when PRx load power is ramping up at the I_{lim} maximum positive slew rate (see § 5.10.3.4.3) between the end of the previous PLA and the middle of the current PLA, the PTx shall not apply power throttling nor disconnect due to FO detection nor shut down. Note: PTx should align its transmitted ITX and power measurements with the TPR

Section	Specification	Description
		power measurements to prevent the above conditions from occurring. The TPR uses $T_{\text{window}} = 32\text{ms}$ and $T_{\text{offset}} = 16\text{ms}$ for its measurement windows (so the PTx should align its measurements to 48ms plus some margin prior to the receipt of the PLA packet preamble). Power throttling may occur for other reasons such as PTx thermal protections.
7.3.2.2.6	PTx MPLA Spec 6	With no FO present, when PRx load power is ramping down at the I_{lim} maximum negative slew rate (see § 5.10.3.5.1) after the middle of the current PLA, the PTx shall not apply power throttling nor disconnect due to FO detection nor shut down. Note: PTx should align its transmitted ITX and power measurements with the TPR power measurements to prevent the above conditions from occurring. The TPR uses $T_{\text{window}} = 32\text{ms}$ and $T_{\text{offset}} = 16\text{ms}$ for its measurement windows (so the PTx should align its measurements to 48ms plus some margin prior to the receipt of the PLA packet preamble). Power throttling may occur for other reasons such as PTx thermal protections.
7.3.2.2.7	PTx MPLA Spec 7	For all TPR positions within the 2x2 cylinder, with no FO present , when delivering 10W to TPR#MPP1(scenario 1) and TPR reports $P_{PR,est} = P_{PR} - 418\text{mW}$, the PTx shall throttle.
7.3.2.2.8	PTx MPLA Spec 8	For all TPR positions within the 2x2 cylinder, with no FO present , when delivering 15W to TPR#MPP1(scenario 2) and TPR reports $P_{PR,est} = P_{PR} - 629\text{mW}$, the PTx shall throttle.
7.3.2.2.9	PTx MPLA Spec 9	For all TPR positions within the 2x2 cylinder, when any Representative Foreign Object is placed on the PTx before external power is applied to the PTx, external power is then applied to the PTx, followed by placement of the TPR on the FO & PTx, and TPR#MPP1 is reporting $P_{PR,est} = P_{PR} + 112\text{mW}$, the PTx shall reduce its power in order to prevent FO heating to a temperature above the limit associated with that object and placement sequence(Scenario 1). Note: If FO flag is used and set, the PTx should limit power delivery (possibly below 15W) to ensure the FO temperature limits are met. The FO detection threshold should be different for FO flag set or cleared (see § 7.3.7 FO Detection Thresholds). P_{FO} should be positive outside the 2x2 cylinder.
7.3.2.2.10	PTx MPLA Spec 10	For all TPR positions within the 2x2 cylinder, after external power is applied to the PTx, when any Representative Foreign Object is placed simultaneously with the TPR on the PTx, and TPR#MPP1 is set to report $P_{PR,est} = P_{PR} + 141\text{mW}$, the PTx shall reduce its power to prevent FO heating to a temperature above the limit associated with that object and placement sequence (Scenario 2).
7.3.2.2.11	PTx MPLA Spec 11	For all positions in the 2x2 cylinder, if no FO is present, the PTx shall send "ACK" or "ATN" to any PLA (0x58) packet from a PRx. Note: Anywhere, the PTx may send "ACK" when an FO is not present or when an FO is present, but the PTx has determined that the FO is not at risk of over-heating at the current power delivery level.
7.3.2.2.12	PTx MPLA Spec 12	If an FO is present, within 8s the PTx shall reduce its transmitted power (by reducing V_{in} or by reducing phase/duty-cycle) to prevent FO over-heating.
7.3.2.2.13	PTx MPLA Spec 13	While the PTx is throttling power due to FO detection, until a new power level is negotiated, the PTx shall send "NAK" to any PLA (0x58) packet from a PRx.
7.3.2.2.14	PTx MPLA Spec 14	While the PTx is throttling power due to FO detection, until a new power level is negotiated, the PTx shall maintain or decrease its equivalent inverter voltage

Section	Specification	Description
		(§ 5.9.4.1). Note: This means that PTx should ignore XCE>0 packets
7.3.2.2.15	PTx MPLA Spec 15	After PTx throttling due to FO detection, if there are no “NAK” events, PTx should negotiate a new power level by sending “ATN” in response to a PLA (0x58) packet from a PRx and update its Power Capabilities to trigger a power negotiation. Note: There should be sufficient PFO margin to ensure that increasing the target power will not lead to FO over-heating. PTx should not send ATN until P_{RECT} as reported in the previous RPP packet is within 200mW of the target level, because if the PRECT is not at the target level PTx cannot judge whether there is sufficient PFO margin.
7.3.2.2.16	PTx MPLA Spec 16	If attempts by PTx to reduce power are not met by TPR in a suitable time (TPR does not negotiate to a new power level with the power capability presented by the PTx), PTx should shut down before FO over-heats.
7.3.2.2.17	PTx MPLA Spec 17	$g_{coil,RX}$ should have a value of 1.0

6.3.2.3 Parameter Representations

When mated, PTx and PRx exchange parameters as indicated in the specifications above and in the Eco-System Scaling section below (Table 7.3.2.3: 21). Here is a list of those variables with their representation and precision.

Table 7.3.2.3: 21 Eco-System Parameter Representation .

Parameter	Representation	Min Value	Max Value	1 LSB
α_{FM}	16-bit two's complement	-16.384 Ω	16.3835 Ω	0.5m Ω
$\alpha_{FM,DC}$	16-bit two's complement	-16.384W	16.3835W	0.5mW
$g_{coil,TX}$	16-bit two's complement	-3.2768	3.2767	0.0001
$g_{coil,RX}$	16-bit two's complement	-3.2768	3.2767	0.0001
PPR	16-bit unsigned	0W	65.535W	1mW

6.3.3 MPLA Equations

As with standard Power Accounting, MPLA estimates the power delivered to an FO by estimating the difference between the power transmitted and the power received:

$$P_{FO} = P_{PT} - P_{PR}$$

where

$$P_{PT} = V_{IN} I_{IN} - P_{circuit\ loss, TX} + P_{coil\ loss, TX} + P_{FM\ loss}$$

which is computed by the PTx, and

$$P_{PR} = V_{RECT} I_{RECT} + P_{circuit\ loss, RX} + P_{coil\ loss, RX}$$

which is computed by the PRx and communicated back to the PTx in PLA packets.